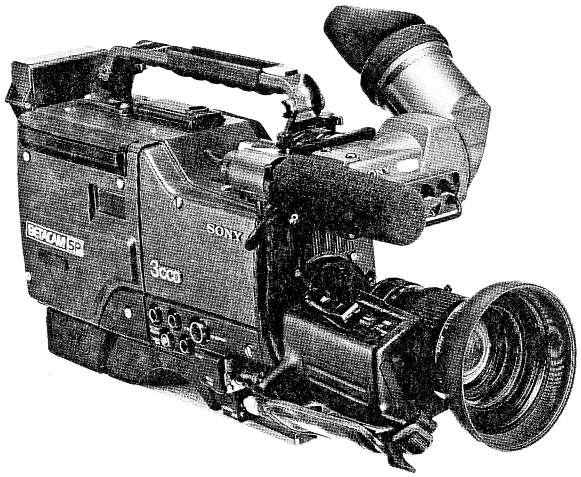
SONY®

VTR IN CAMERA

# BVW-300P




BETACAM SP™

## THEORY OF OPERATION

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# CAMERA BLOCK

# SECTION 1
# GENERAL

## 1-1. OUTLINE OF CAMERA BLOCK

### 1-1-1. CCD Drive System

**TG-57 Board**
The TG-57 board has functions to feed CCD drive pulse to the DR-84 board and CCD output sampling pulse to the PA-101 board. The CCD drive pulse becomes synchronized with the sync signal that is generated by the SG-152 board, and is sent to the DR-84 board. The TG-57 board sends also 908fH signal to the SG-152 board.

**DR-84 Board**
The DR-84 board converts the CCD drive pulse input that is supplied from the TG-57 board, to the appropriate forms of pulse that are suited to drive CCD unit directly. The converted pulses are sent to CCD unit via the BI-22 board, BI-23 board and BI-24 board. The DR-84 board has also the power regulator circuit that generates +29V output from +15V input.

**BI-22/23/24 Boards**
CCD unit is installed on the BI boards. The CCD drive pulses and control dc voltages are supplied to CCD unit via the BI boards. Video output signal from CCD unit is buffered and then sent to the PA-101 board.

**PA-101 Board**
The PA-101 board has function to remove pulse component from the video output signal that is supplied from the BI board. The processed video signal after noise removal is clamped of its black level, is shifted its time base for the amount of 1/2 pixel for resolution improvement, amplified by preamplifier and is sent to the VA-83 board.

### 1-1-2. Video Signal System

**VA-83 Board**
The VA-83 board has function of video signal processing for the PA-101 board output video signal, such as amplification, black shading correction, gain-up, blanking cleaning and white shading correction. Selection of either main video signal or TEST SAW signal is also performed.

**IE-20A Board**
The IE-20A board has function of generating image enhancing detail signal from the G and R video signals that are supplied from the VA-83 board, for increasing resolution power. The detail signal is sent to the PR-132 board where it is added to the main line R/G/B video signals. Only the G video signal is delayed for 1H period in the IE-20A board, and then sent to the PR-132 board.

**PR-132 Board**
The PR-132 board has the signal processing function to the respective R/G/B signals, such as masking signal addition, detail signal addition, flare compensation, pedestal control, knee correction, white clipping and gamma correction. The signal after processing is sent to the EN-79 board.

**EN-79 Board**
The EN-79 board has signal encoding function that generates Y (luminance) signal, chroma (R−Y, B−Y) signal and composite video (VBS) signal from the PR-132 board's output R/G/B signals. The EN-79 board generates also EBU color bar signal.

### 1-1-3. Power Supply System

**CD-89 Board**

The CD-89 board has function of generating the power voltages that are needed in each board, such as ±9V, ±5V and switched +6V dc from the externally supplied dc power (unregulated) by switching regulator. The CD-89 board gives also other power voltages such +9.3V (viewfinder power), +15V/+7V (CCD control voltage) and +48V (microphone phantom power). The power voltages of switched +6V, +15V, +7V and +48V are on/off controlled by the control signals that are supplied from system control circuit in accordance with operating mode of this equipment.

### 1-1-4. Sync Signal System

**SG-152 Board**

The SG-152 board consists of sync signals generator circuit generating various sync signals, external sync lock circuit by automatically detects externally supplied gen-lock signal, auto-iris circuit to control lens iris automatically by detecting video output signal level, power regulators of +8.5V/+4.6V/−4.5V that are sent to video signal circuit and auto operation related circuit and power regulator that generates CCD drive +4.7V from +9V/+5V/−5V that are supplied from the CD-89 board.

### 1-1-5. Auto Operation System

**AT-49A Board**

A microcomputer is installed in the AT-49A board that generates various control signals and correction signals to respective circuit board in accordance with the commands that are supplied from each function keys. Position of color temperature conversion filter, and master pedestal level and video level are automatically detected to generate various correction signals and alarm signals. The interface circuit between a camera and remote control RM-P3, and the audio level detection circuit for audio level display are also installed in the AT-49A board.

# SECTION 2
# CCD IMAGE SENSOR

## 2-1. OUTLINE

A CCD (Charge-Coupled Device) image sensor is a semiconductor device consisting of a large number of unit cells regularly laid-out in two dimensional arrays. It has the following three functions :

1. Photo-Electric Conversion
When incident light falls on the image sensor, the photo-charge is generated in proportion to the illumination received.

2. Photo-Charge Storage
When an external voltage is applied to the electrode of a charge-coupled element or unit cell, a "potential well" is generated in the silicon substrate of the unit cell which can store the accumulated photo-charge.

3. Photo-Charge Transfer
When voltage is successively applied to the electrodes of adjacent cells, the photo-charge can be transferred sequentially from one unit cell to an adjacent cell.

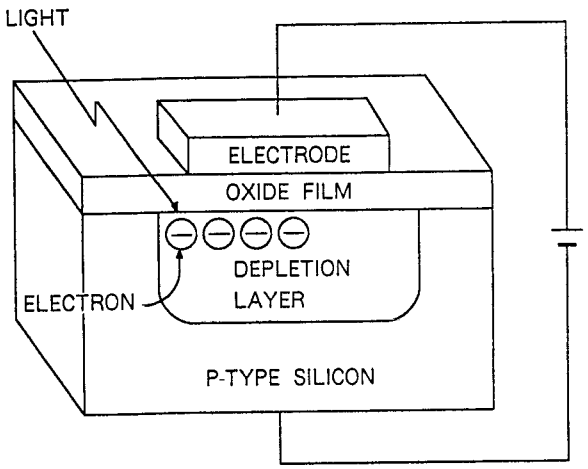



**Fig. 2-1. Unit Cell (MOS Capacitor)**

## 2-2. STRUCTURE OF CCD IMAGE SENSOR

### 2-2-1. Number of Effective Picture Elements

The SONY ICX-034 CCD image sensor is used in this equipment. The ICX-034 CCD imager consists of 816 elements horizontally and 606 elements vertically. Of the total number of sensor elements, 30 horizontal elements (5 elements at the beginning and 25 elements at the end), and 25 vertical elements (6 elements at top and 19 elements at bottom) are optically masked to generate the optical black reference level. The total number of effective picture elements is 786 elements (horizontally) ×581 elements (vertically).

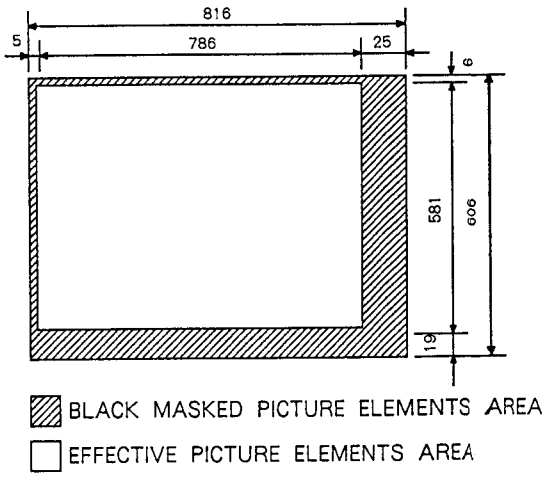



**Fig. 2-2. Number of Effective Picture Elements**

### 2-2-2. Internal Structure of the CCD Imager

A CCD imager consists of the following four functional blocks :

(1) Photo-sensor
The photo-sensor block converts the illumination on the photo-site into a photo-charge (illumination-to-electric signal conversion). The photo-charge accumulated during the sensing interval is stored in this photo-sensor element.

(2) V (Vertical Transfer) Register
A photo-charge packet generated in the photo-sensor block is moved vertically by the charge-transfer (charge-coupling) characteristic of the vertical register. The photo-charge is thus shifted vertically to the H (horizontal) register block.

(3) H (Horizontal Transfer) Register
The photo-charge supplied from the V register is moved horizontally to the output stage by the H register.

(4) Output Stage
The photo-charge from the H register is converted from an electric charge into voltage at the output stage. The signal voltage is amplified and sent to external circuits.

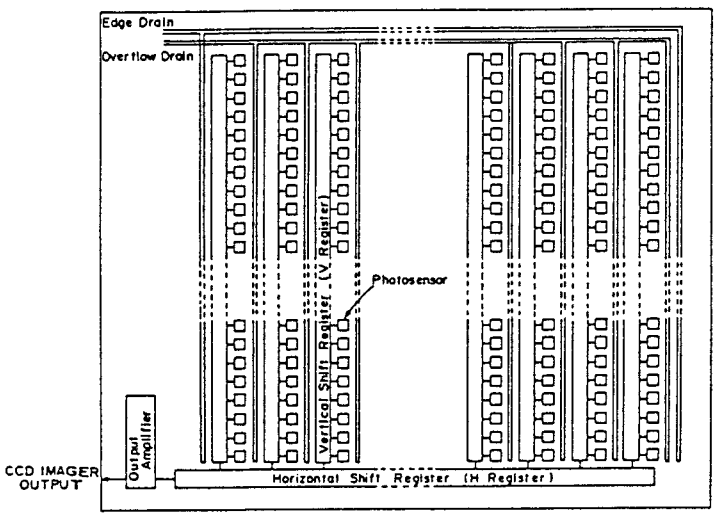



Fig. 2-3. Internal Structure

### 2-2-3. Structure of the CCD (ICX-034)

ICX-034 is a 2/3-inch interline transfer CCD. Tables 2-1 lists its specifications.

| | |
|---|---|
| CHIP SIZE | 10.0 (H) ×8.2 (V) mm |
| SENSITIVE SIZE | 8.8 (H) ×6.6 (V) mm |
| SENSITIVE PIXEL NUMBER | 786 (H) ×581 (V) |
| READ OUT CLOCK RATE | 14.75 MHz (4fsc=944fH) |
| UNIT CELL SIZE | 11 (H) ×11 (V) μm |
| SENSOR APERTURE RATIO | 34% (49 $\mu m^2$) |
| SENSOR STRUCTURE | HADS (HOLE ACCUMLATED DIODE SENSOR) |
| O.F.D. STRUCTURE | VERTICAL O.F.D. |

Table 2-1.

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | V4 | Vertical register transfer clock |
| 2 | V3 | Vertical register transfer clock |
| 3 | V2 | Vertical register transfer clock |
| 4 | SUB | Substrate (OFD) bias |
| 5 | GND | GND |
| 6 | V1 | Vertical register transfer clock |
| 7 | VL | Protective transistor bias |
| 8 | NC | |
| 9 | NC | |
| 10 | $V_{DD}$ | Supply voltage |
| 11 | $V_{OUT}$ | Signal output |
| 12 | Vcc | Output amplifier gate |
| 13 | Vss | Output amplifier source |
| 14 | GND | GND |
| 15 | PD | Precharge drain bias |
| 16 | PG | Output reset clock |
| 17 | VL | Protective transistor bias |
| 18 | H2 | Horizontal register transfer clock |
| 19 | H1 | Horizontal register transfer clock |
| 20 | GND | GND |

Table 2-2.

[Functional blocks]

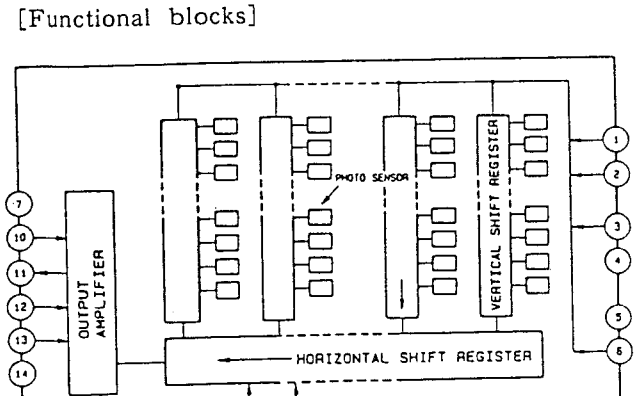



**Fig. 2-4. Function Block**

[Internal structure]

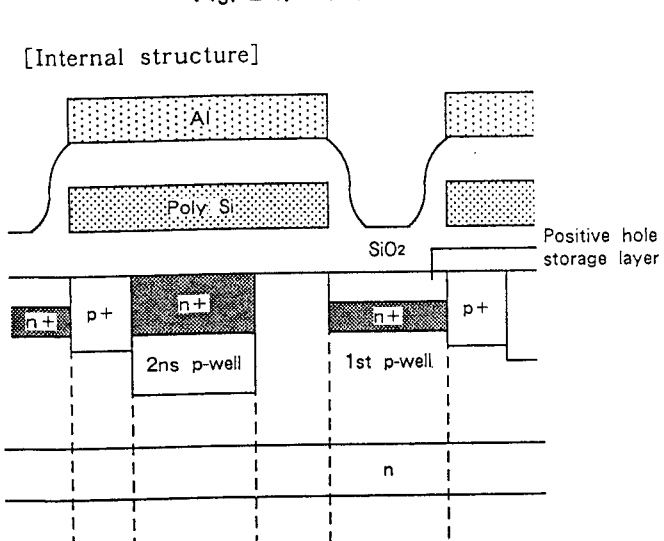



**Fig. 2-5. Cross Section of ICX-034**

ICX-034 contains a photoelectric converter consisting of photodiodes and positive hole storage layers, a readout gate region, horizontal and vertical shift registers consisting of an n-type buried-channel CCD, and an output amplifier.

ICX-034 uses n-type substrate and p-well structure. The second p-well is provided under the V register to suppress smear.

The sensor has n+p diodes provided with a positive hole storage layer in order to increase sensitivity and decrease dark current.

## 2-3. PRINCIPLE OF ELECTRONIC SHUTTER

CCD is a device that converts incoming light into electric signal, charges temporarily the resultant pixel output internally into well, and reads-out the charged signal to generate its video output. So, by changing the charging time, the same effect as shutter in an ordinary still film camera can be obtained in CCD electronic camera.

CCD normally charges pixel output during the period of 1/50 seconds that is specified by television standard. In case of electronic shutter, pixel output is charged only during the period of specified shutter speed (for example, 1/2000 second, 1/1000 second ···) so that it enables to shoot a fast moving object clearly as shown in Fig. 2-6.

The CCD that is used in this equipment has vertical type over-flow drain (VOFD) structure which throws away excessive charge (over-flow charge) in the direction of depth of CCD chip. Barrier is built by giving dc bias to the VOFD from external source. As shown in Fig. 2-8, the signal charge can be stored with the barrier. If barrier should not exist, the signal is thrown away. Electronic shutter is realized by changing the period of time during which the barrier exists. In other word, charging time is 1/50 second in normal operation while the charging time is shortened in electronic shutter mode during which signal charge is stored. Signal charge is thrown away all the rest of time.

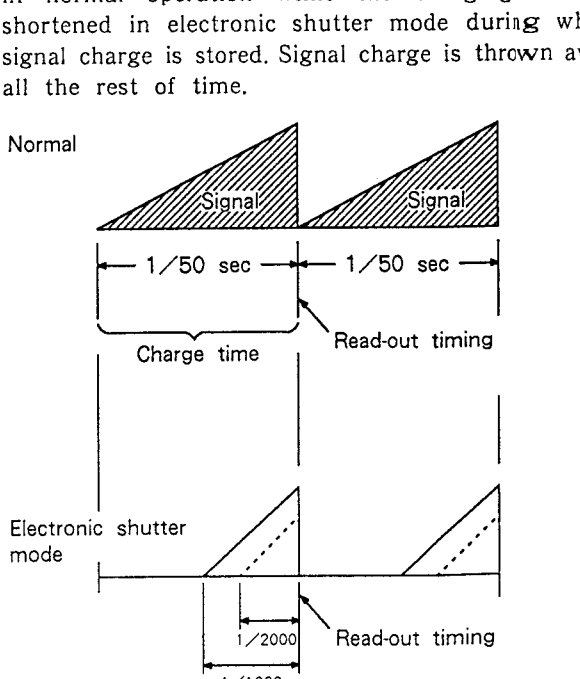



**Fig. 2-6. Electronic Shutter**

In this unit, the charge discarding pulse that is synchronized with horizontal blanking is mixed with the dc bias of VOFD as shown in Fig. 2-7. Thus electronic shutter is realized. This electronic shutter system is capable of changing shutter speed from 1/50 second to 1/15625 second with every 1/15625 second step : .

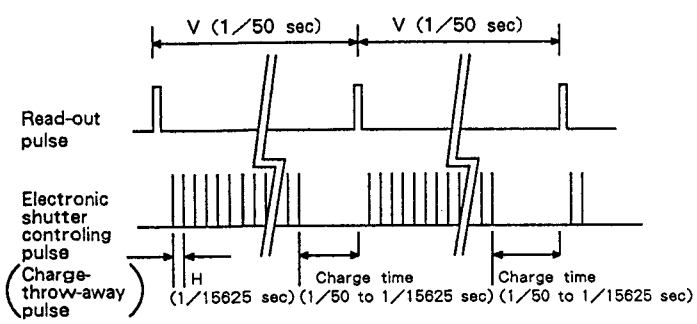



**Fig. 2-7. Charge Discarding**

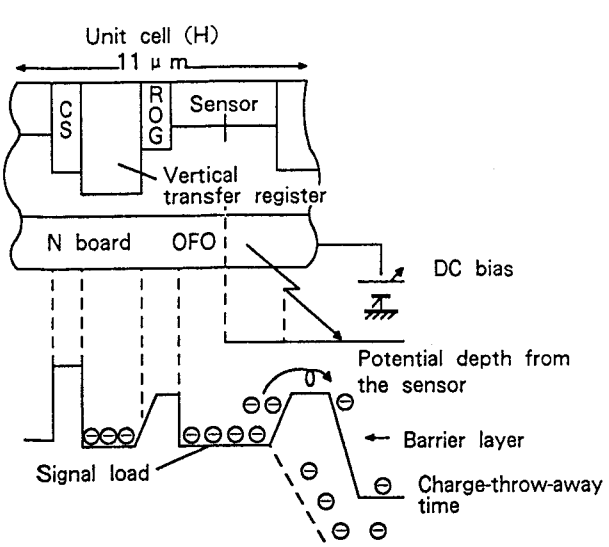



**Fig. 2-8. Construction of VOFD**

## 2-4. V REGISTER

### 2-4-1. Structure of the V Register

The vertical register has the following blocks :

(1) ROG (Read-Out Gate)
The ROG controls operation of the V register which reads the photo-charge from the image sensor. The voltages V1 and V3 in Fig. 2-9 are also controlled by the ROG.

(2) OFCG (Over-Flow Control Gate)
The excessive photo-charge caused by extremely high incident light at the sensor, overflows to limit peak signal amplitude.

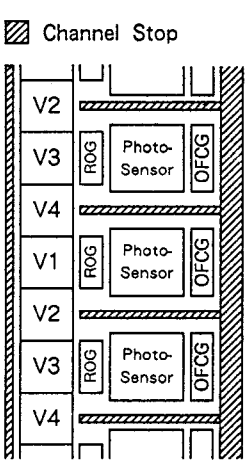



**Fig. 2-9. Structure of the V Register**

### 2-4-2. V Register Operating Principle

The V register operates on a "three-value, four-phase" drive system which reads the signal photo-charge from the photo-sensor element. It also transfers the photo-charge to the H register.

#### (1) "Three-value, Four-phase" Drive System

The photo-charge is moved by the "four-phase" drive system of the V register as shown in Fig. 2-10. The bias voltages applied to the electrode (potential well) are switched in the sequence shown below so that the photo-charge is shifted from the photo-sensor element to the H register.

| STEP | TIMING | POTENTIAL (VOLTAGE) |
|---|---|---|
| 1 | t0 | INITIAL CONDITION |
| 2 | t1 | V3 DOWN (UP) |
| 3 | t2 | V1 UP (DOWN) |
| 4 | t3 | V4 DOWN (UP) |
| 5 | t4 | V2 UP (DOWN) |
| 6 | t5 | V1 DOWN (UP) |
| 7 | t6 | V3 UP (DOWN) |
| 8 | t7 | V2 DOWN (UP) |
| 9 | t8 | V4 UP (DOWN) |

**Table 2-3. "Three-value, Four-phase" Drive System**

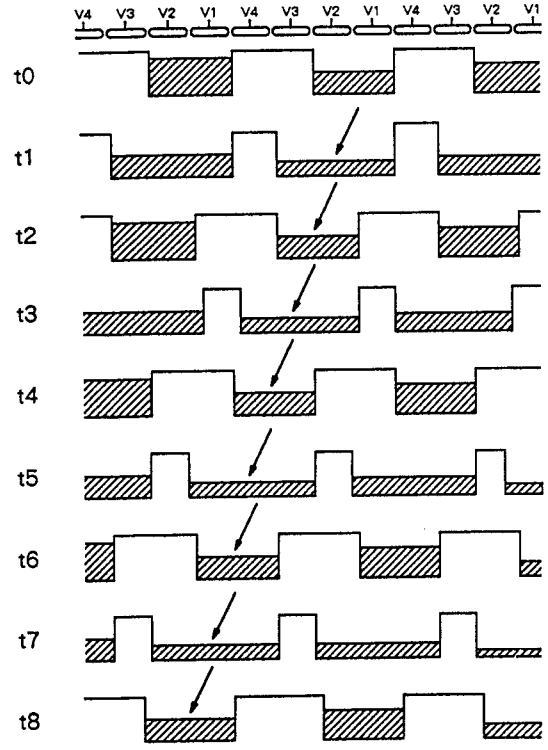



**Fig. 2-10. Photo-charge Transfer Operation**

#### (2) Signal Charge Read-out

The signal charge is read-out from the photo-sensor field-by-field (or frame-by-frame). As shown in Fig. 2-11, when the signal charge is transferred, the V register's potential stays at either levels ① or ②. When the V register's potential attains level ③, the signal charge is read-out from the photo-sensor. The signal charge stored in the photo-sensor is simultaneously moved to the V register.

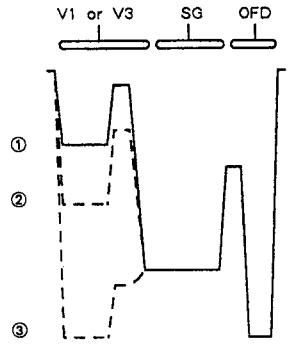



**Fig. 2-11. Signal Charge Read-out**

## 2-5. H REGISTER

### 2-5-1. Structure of the H Register

Fig. 2-12 shows the relation between the structure of the H register and potential levels. As shown in Fig. 2-12, the V register is connected to H1 of the H register.

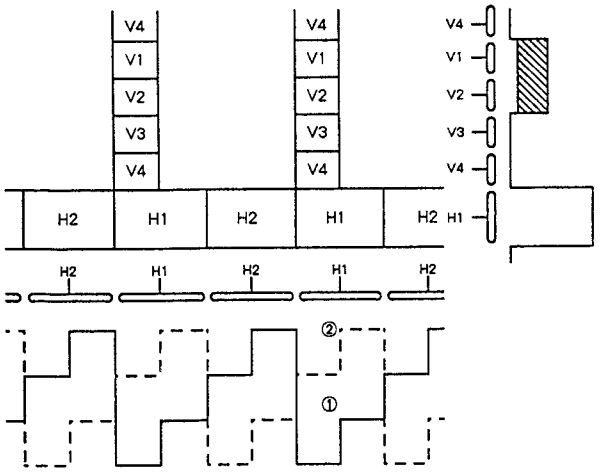


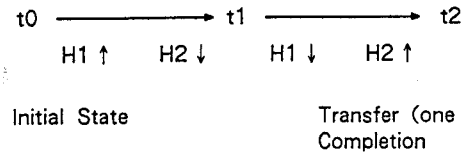

Fig. 2-12. Structure of the H Register

### 2-5-2. H Register Operating Principle

The H register receives the signal charge from the V register and transfers it in a horizontal direction to the output block, employing the two-phase drive system.

#### (1) Two-phase Drive System

Operating principle of the two-phase drive system used for transferring the signal charge is described in Fig. 2-13.



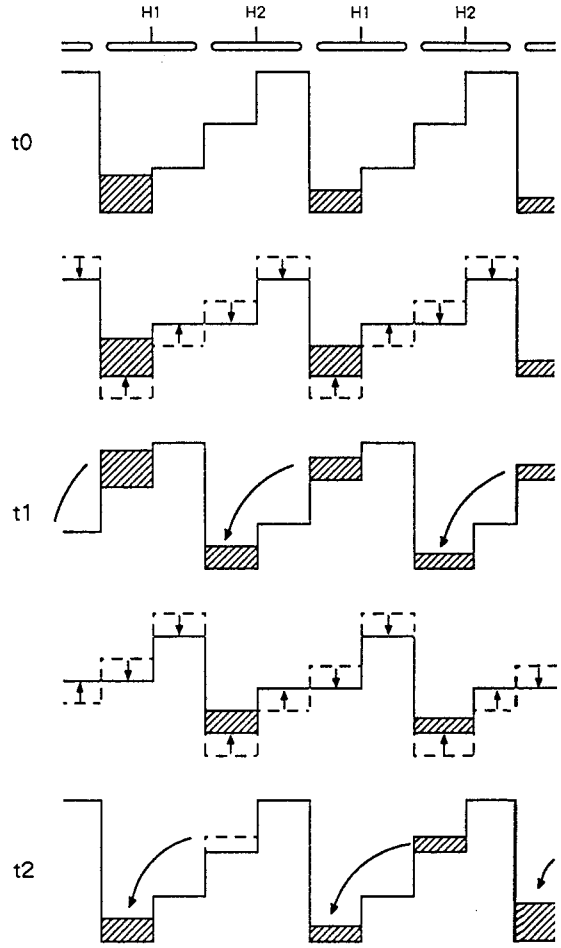




Fig. 2-13. Two-phase Drive System

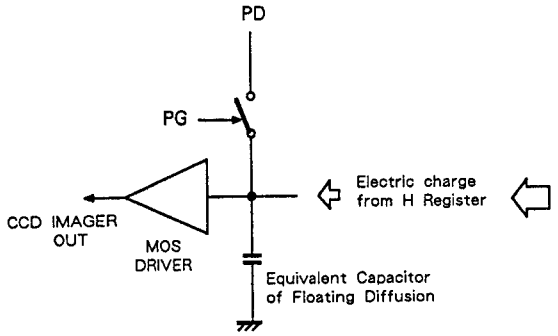
#### (2) Signal Charge Transfer

Signal charge transfer from the V register to the H register takes place during the horizontal blanking period. As shown in Fig. 2-12, the H register maintains either potential level ① or ② during the signal charge transfer period. The charge transfer is completed during the horizontal blanking period. H1 reaches level ①, which is lower than at V4.

While the H register is transferring a signal charge, the V register stops signal transfer. At this time, the V1 and V2 potentials are lower and V3 and V4 potentials are shallower, so the signal charge is stored in V1 and V2. As soon as the H register has completed signal transfer, the V register starts its signal transfer so the signal charge is sent to the H register (see Fig. 2-10).

### 2-5-3. Output Block

The output block consists of the equivalent circuits shown in Fig. 2-14.



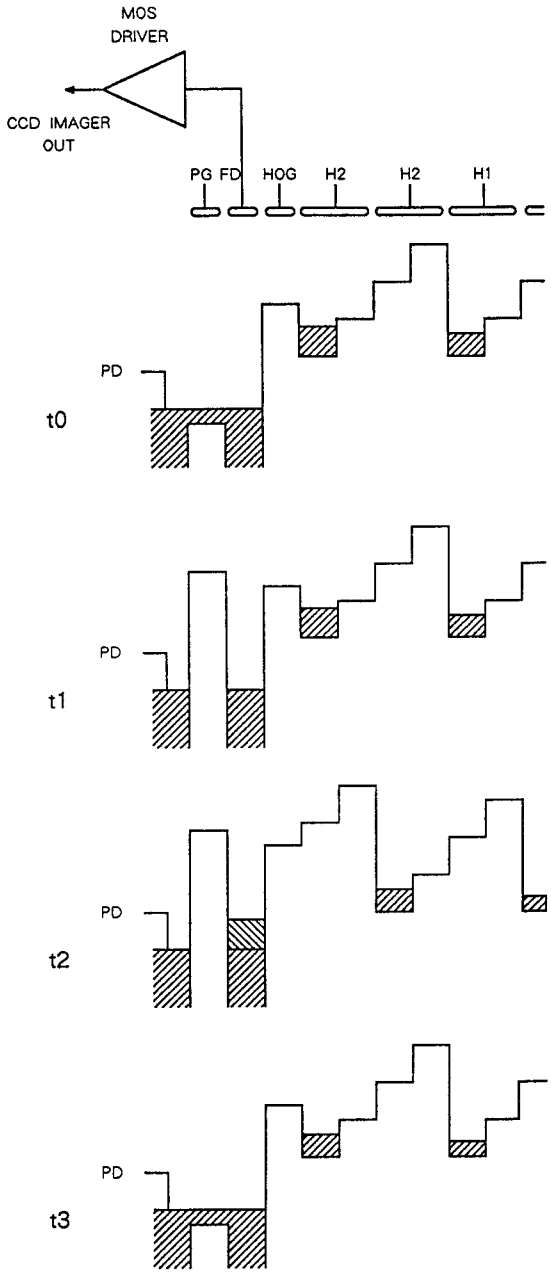




Fig. 2-14. Output Block Equivalent Circuit

- t0 : The PG (Precharge Gate) remains in the ON state so the FD (Floating Diffusion) is reset to the PD (Precharge Drain) potential.
- t1 : The PG is set to OFF.
- t2 : The H1 potential becomes shallow and the H2 potential becomes deep so the charges stored in H1 are sent to HOG (Horizontal Output Gate) and then to the FD (Floating Diffusion ) where the signal charge is converted to the signal voltage (V=Q/C) by equivalent capacitance of the FD.
- t3 : The PG is turned ON so that the FD is reset to the PD potential.

Through these operations of t0 through t3, the signal charge is converted to a signal voltage amplified by the MOS driver and is sent to the external circuit as a CCD image signal (Fig. 2-15).

Fig. 2-15. CCD Output Signal

# SECTION 3
# CCD BLOCK

## 3-1. OUTLINE

The CCD block consists of the following printed circuit boards :

- TG-57
- DR-84
- CN-273
- BI-22
- BI-23
- BI-24
- PA-101

## 3-2. TG-57 BOARD

### 3-2-1. OUTLINE

The TG-57 board generates the timing pulses to drive the CCD arrays and the other timing pulses needed for sampling the CCD imager output signal. These timing pulses are generated by IC11.
Mode of timing pulses generated by IC11, are determined by the data output from ROM IC7.

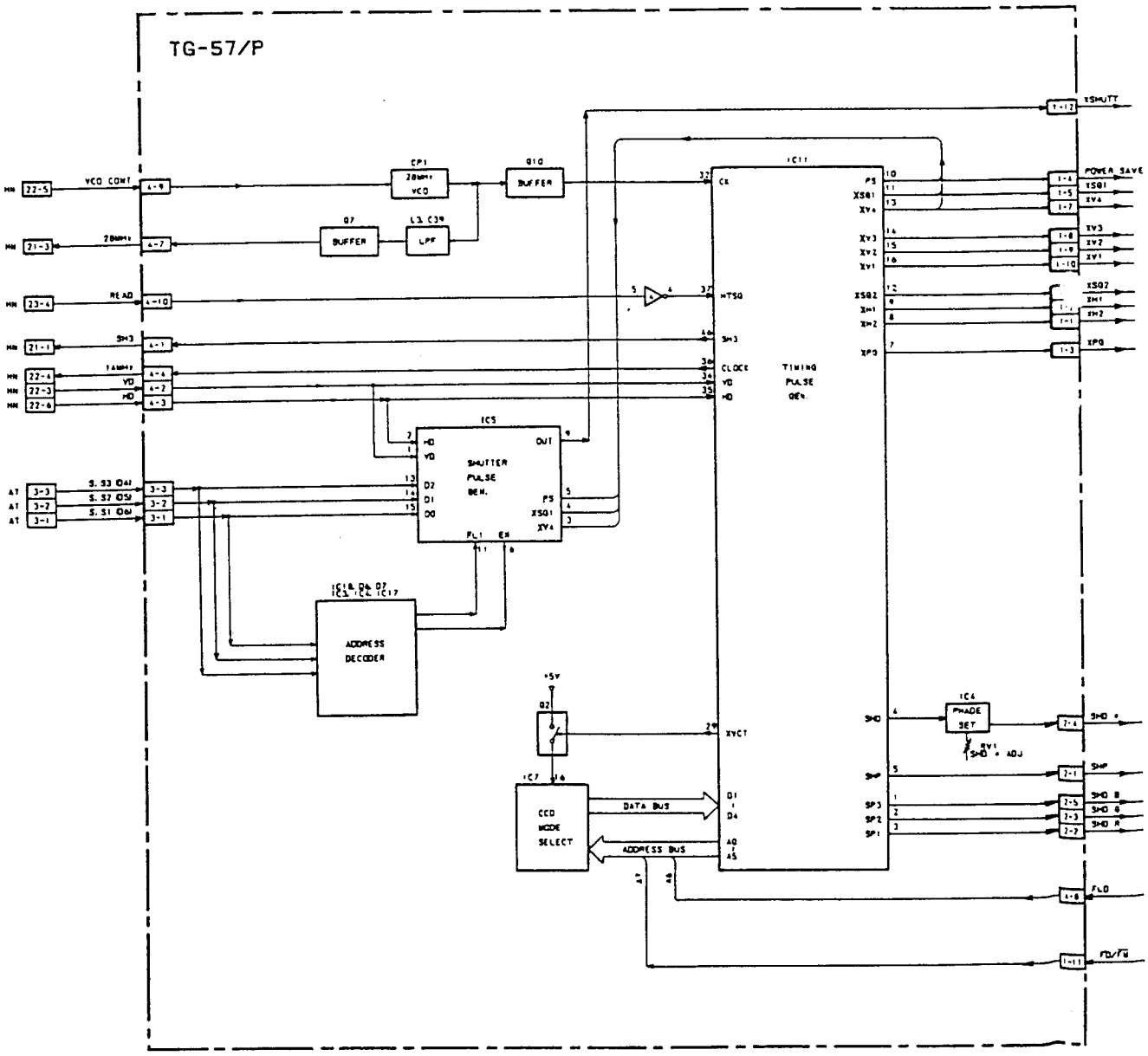
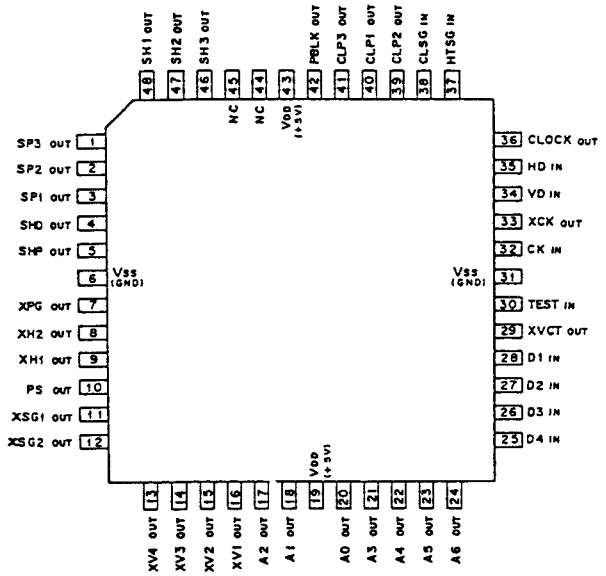
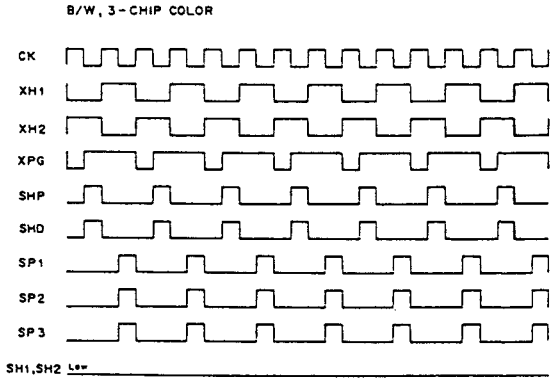



Fig. 3-1. TG-57 Board Block Diagram

## 3-2-2. Specifications of IC1 (CXD1035BQ-Z) and IC7 (MB7114L)

CXD1035BQ-Z (SONY) FLAT PACKAGE
C-MOS TIMING PULSE GENERATOR FOR CCD CAMERA
— TOP VIEW —




MODE SELECTION WITHOUT ROM

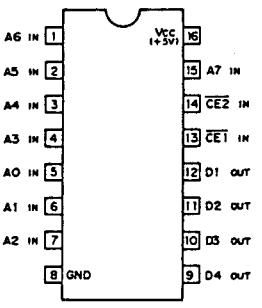
| | HIGH (VDD) LEVEL | LOW (VSS) LEVEL |
|---|---|---|
| D1 | * | |
| D2 | 1-CHIP COLOR | B/W, 3-CHIP COLOR |
| D3 | FRAME | FIELD |
| D4 | EIA (NTSC, PAL-M) | CCIR (PAL, SECAM) |

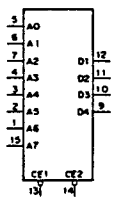
* Connect D1 to GND without ROM (ROM OFF)

D1 – D4 : EXTERNAL ROM DATA INPUT
A0 – A6 : EXTERNAL ROM ADDRESS OUTPUT

Fig. 3-2. IC1 (CXD1035BQ-Z)

MB7114LPF (FUJITSU) (ACCESS TIME = 50nS) FLAT PACKAGE
1024-BIT (256x4) PROM
— TOP VIEW —




A0–A7 ; ADDRESS INPUTS
D1–D4 ; DATA OUTPUTS
$\overline{CE1}$, $\overline{CE2}$ ; CHIP ENABLE INPUTS

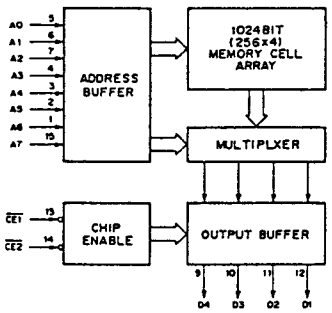



Fig. 3-3. IC7 (MB7114L)

## 3-2-3. Timing Chart of IC1 (CXD1035BQ-Z)

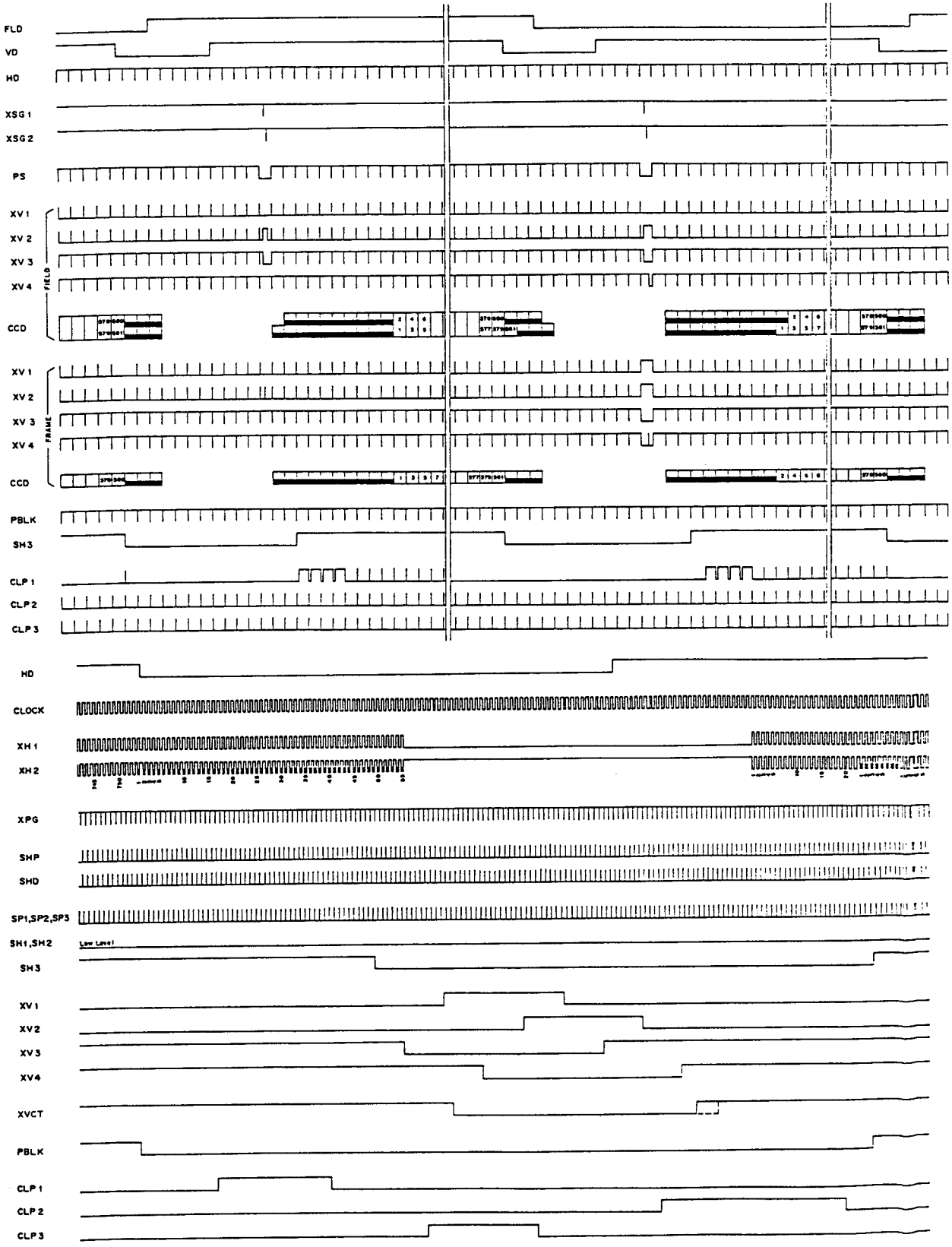



Fig. 3-4. Timing Chart of IC1 (CXD1035BQ-Z)

### 3-2-4. Field Transfer System

The BVW-300P employs the field transfer system to read the signal charge from the CCD imager. In the field transfer system, the signal charges stored in the photo sensors inside the CCD are read-out at V1 or V3 of the V register connected to the photo sensors. All the signal charges of one entire field are shifted simultaneously to the V register in the field transfer system.

During odd field scanning, the V2 potential becomes lower so the signal charges from V1 and V3 are added and transferred.

During even fields, the V4 potential becomes lower so the signal charges from V3 and V1 are added and transferred.

As shown in Fig. 3-5, the combination of signal charged from the odd field and even field is alternated as shown by the oblique lines of Fig. 3-5. Each single section of a photo sensor cell has a dynamic range of approximately 300%. By adding the output of two photo sensor cells, approximately 600% dynamic range is realized.

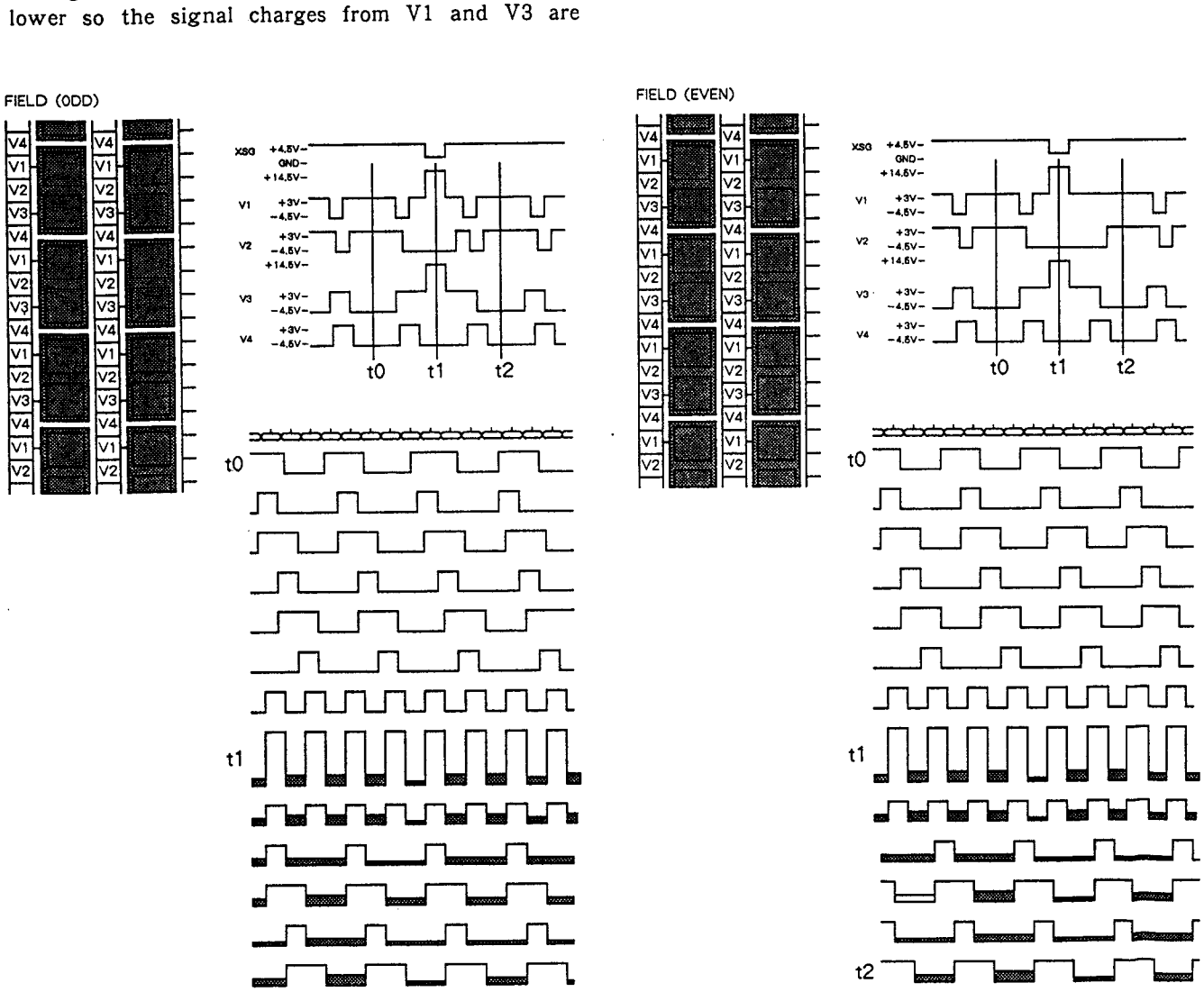



Fig. 3-5. Field Transfer Timing

### 3-2-5. Spatial Phase Correction Circuit

This equipment employs "sensor elements spatial offset" technology to improve the picture resolution. Spatial offset technology displaces the physical position of the G-channel CCD imager with respect to that of the R-/B-channel CCD imagers by exactly 1/2 pixel. This spatial (physical) displacement of imagers detects the information between pixels inside the CCD imager.

For example, when an object (Fig. 3-6) is shot by the imager, the object is focused on the sensing planes of the G-channel and R-/B-channel imagers. The A and B portion of the object are shown enlarged in Fig. 3-7 (A) and (B). Because the G-channe l photo sensor is located between the photo sensors of R-/B-channel (V register area), the photo sensors of respective channels have an accumulated photo charge (signal level) as shown by ① through ⑦ of the illustration.

Fig. 3-7 (A') and Fig. 3-7 (B') indicate the photo charge (signal level) when spatial offset technology is not employed.

Fig. 3-7 (C) illustrates the addition of (A') and (B') when spatial offset is used. It shows that the picture resolution power of (C) is improved over (B') and (A'). Because the G-channel image sensor is installed at an offset of 1/2 pixel with respect to R-/B-channel image sensors, the G-channel output signal has phase error with respect to the R-/B-channel output signals. This phase error is corrected by the spatial phase error compensation circuit.

The G-channel output signal is once sampled/held by the CDS circuit at the pre-charge and data level of the output signal. This signal is sampled again by the SHD $\pi$ pulse with a spacial delayed phase equal to the offset. Thus the delayed pre-charge and data levels are supplied to the differential amplifier inputs. The output signal of the differential amplifier is therefore phase-compensated by this delay.

The SHD $\pi$ pulse is the spatial offset phase correction signal supplied from the TG-57 board. Adjustment RV1 (SHD $\pi$ PHASE adj.) of the TG-57 board provides phase error correction. By adjusting the phase of the SHD $\pi$ pulse, the G-channel delay time can be varied.

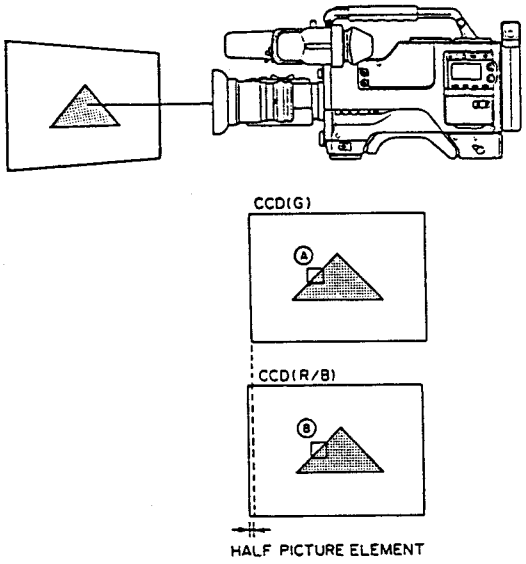



Fig. 3-6. Spatial Phase Adjustment (1)

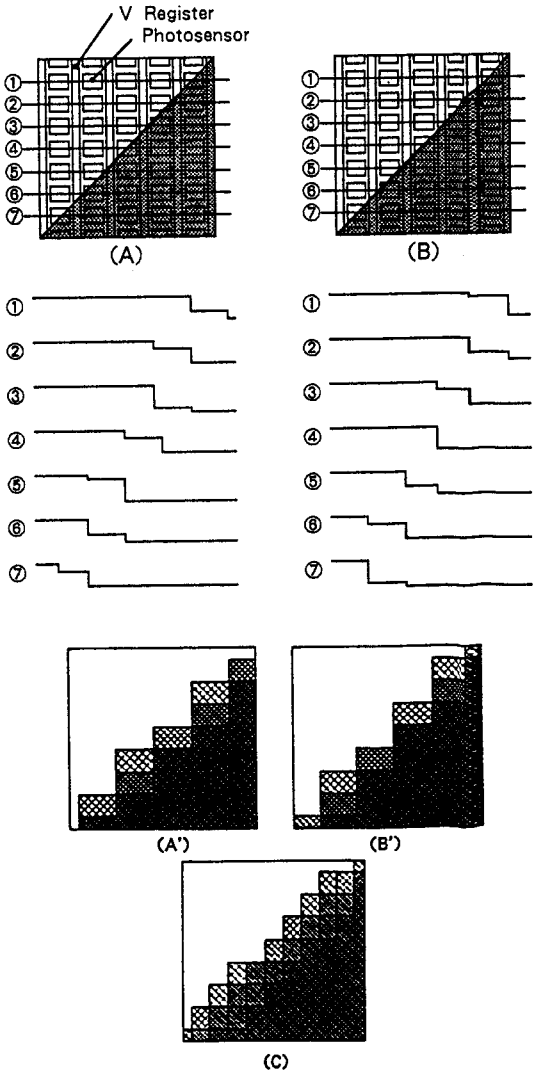



Fig. 3-7. Spatial Phase Adjustment (2)

## 3-3. DR-84 BOARD

### 3-3-1. CCD Drive Signal Output Circuit

In order to drive vertical register of CCD directly, the timing pulse that are prepared by the TG-57 board is converted to driving clock pulse by IC1 (B channel), IC2 (G channel) and IC3 (R channel). The driving clock pulse is sent to the BI board via the CN-273 board so that vertical register of CCD is driven by IC1 of the BI board.
IC1, IC2 and IC3 have built-in power save function that puts these ICs into power save mode when vertical register does not transfer signal charge.
Timing pulse to drive horizontal register of CCD that is supplied from the DR-84 board directly to the CN-273 board, is separated into respective R/G/B channel, phase-inverted, and drives horizontal register of CCD through the BI board IC1.
Voltage of level of PG pulse that is supplied from the TG-57 board, is determined by buffer (Q2, Q3) and sent to driver (Q4, Q5) and series regulator (Q1). The PG pulses with voltage levels are sent to respective R.G.B channel in the CN-273 board and then to the BI board to drive CCD. VL (−12V) voltage that is output from IC1 is bias voltage for CCD protection diode.
The SHUTT signal that is supplied from the TG-57 board is buffered by Q9 and is separated into SHUTT (+) signal and SHUTT (−) signal by Q10. The SHUTT (+) signal passes through driver Q11 and Q12. The SHUTT (+) and SHUTT (−) signals are sent to the CN-273 board where they are separated into respective R.G.B. channel and are sent to the BI board to drive CCD.
The DR-84 board has built-in power sub-regulator to convert +15V into +29V.

### 3-3-2. Sub-Regulator

Sub-regulator generates V-sub voltage from +29V using +5V as reference voltage. The optimum voltage value of the V-sub voltage is not a fixed value, but some value in the range from +9 Vdc to +19 Vdc, depending upon characteristics of each CCD unit. The V-sub voltage of respective R.G.B channel is determined by RV1, RV2 and RV3. If the V-sub voltage is set too low, gate potential of CCD's VOFD becomes shallow that can cause blooming or smear. If the V-sub voltage is set too high on the contrary, gate potential of VOFD becomes too deep that can prevent CCD from blooming or smear but 600% dynamic range becomes difficult to obtain.

## 3-4. BI-22/23/24 BOARDS

The CCD unit is installed on the BI boards. The CCD drive clock signal and other various dc bias voltages are sent to the CCD unit.
The output video signal from the CCD unit is buffered by Q1 and sent to the PA-101 board.

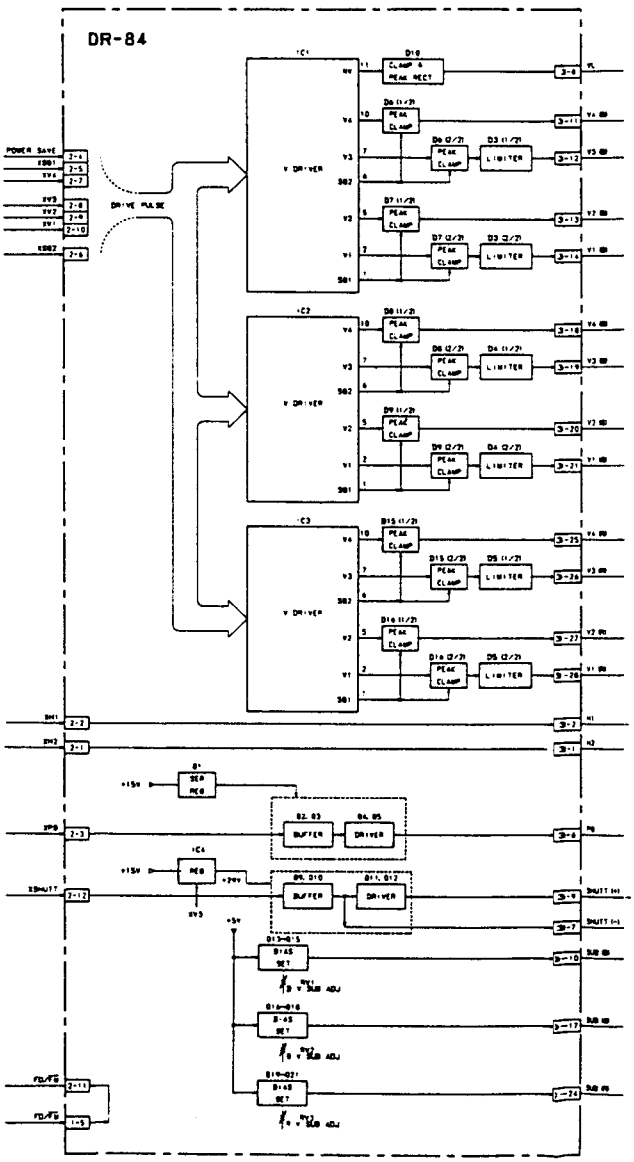



Fig. 3-8. DR-84 Board Block Diagram

## 3-5. PA-101 BOARD

PA-101 board has correlated double sampling circuits for R.G.B. channels. Because CCD output video signal includes inherent noise, the major noise component is designed to be removed by the correlated double sampling circuit in the PA-101.

### 3-5-1. Correlated Double Sampling Circuit

This circuit consists of following circuits.
- Signal sample and hold circuit
- Pre-charge level sample and hold circuit
- Differential amplifier
- Green channel SHD $\pi$ sample and hold circuit

(1) Signal Sample and Hold Circuit
Red channel CCD output signal that is supplied from pin 2 of CN6 is divided to two outputs. One output is sent to the pre-charge level sample and hold circuit. The other output is buffered by Q7 and is sampled and held by Q8. Sample and hold of data is activated by SHD pulse that is supplied from the TG-57 board. Q8 output signal is buffered by Q9 and is sent to inverting ; input (−) pin of differential amplifier Q10 through Q13.

(2) Pre-charge Level Sample and Hold Circuit
After buffered by Q1, red channel CCD signal is sampled and held by Q2. The sample and hold is activated by SHP (Sample and Hold of Pre-charge level) pulse.
Subsequent sample and hold for CCD signal is activated at Q5 using the SHD as mentioned before, for the purpose of maintaining a constant signal phase. The sample and hold output is sent to differential amplifier (Q10 through Q13) where noise is removed from CCD signal.

(3) Differential Amplifier
The differential amplifier consists of Q10 through Q13 that extracts video signal component and at the same time removes in-phase noise component. Clock-coupling induced by sample and hold is also removed by differential amplifier. Amplification gain of the differential amplifier can be set by RV1 (Red Streaking Adj.).

(4) Green Channel SHD $\pi$ Sample and Hold Circuit
It consists of Q50 and Q53. Since green channel signal phase advances for 180 degrees to that of R/B channel due to spatial displacement system. This circuit uses SHD $\pi$ pulse whose phase is advancing for 180 degrees so that the green channel signal phase is delayed for 180 degrees.

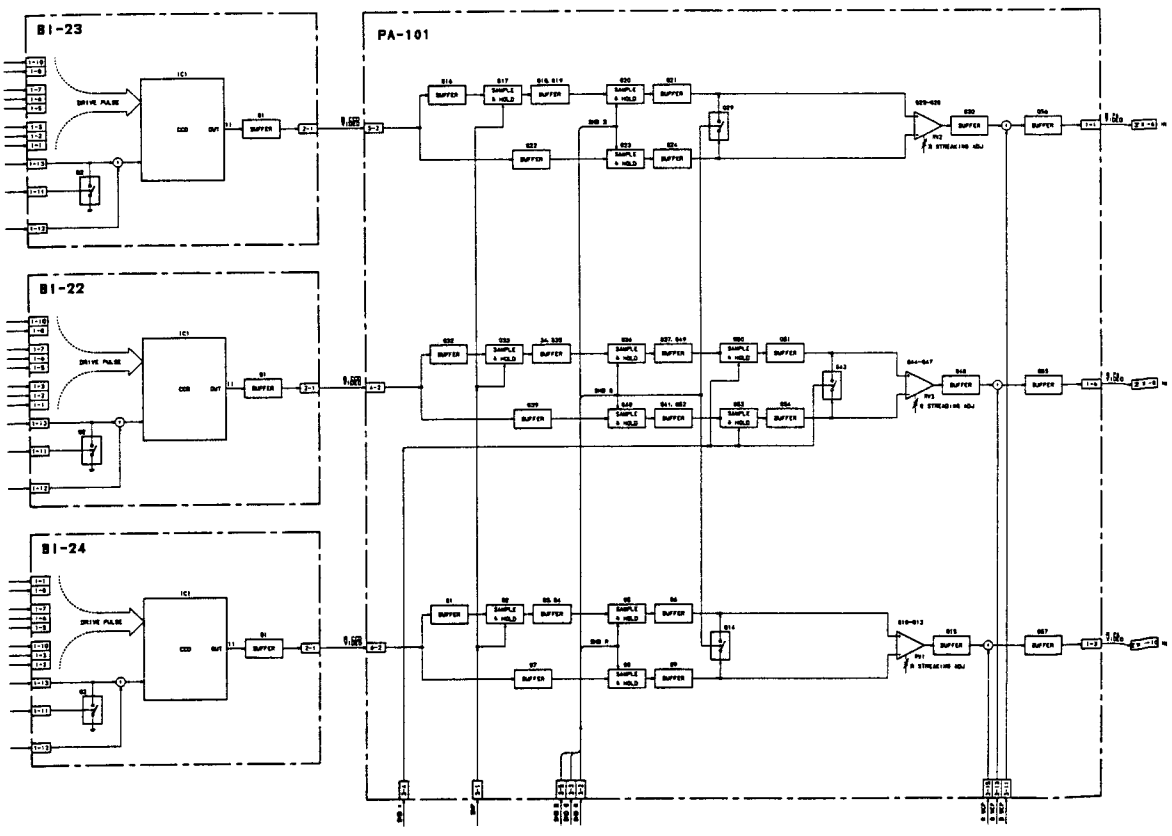



Fig. 3-9.

# SECTION 4
# VA-83 BOARD

## 4-1. OUTLINE OF VA-83 BOARD

The VA-83 board has function of video signal processing as listed before to be applied to R/G/B signals that are supplied from pre-amplifier on the PA-101 board. Output video signals after processing are sent to the PR-132 board.

- Video amplifier gain switching
- Blanking cleaning
- Gain control
- Pre-knee correction
- Horizontal shading correction waveform generator
- Vertical shading correction waveform generator
- Black shading correction waveform generator
- White shading correction waveform generator

## 4-2. VIDEO AMPLIFIER GAIN SWITCHING CIRCUIT

Since R, G and B channels have identical circuit, only B channel is explained.

The VA-83 board receives B channel input with approximately 50 mVp-p from the PA-101 board at the reference signal level (at 2000 lux/F5.6/3200° K). The G channel input has 155 mVp-p and R channel input has 90 mVp-p signal level. These input signal levels may vary depending upon characteristics of CCD unit.

The input B channel signal is sent to band-elimination filter FL3 where 14 MHz sampling frequency component is removed. The FL3 output signal is amplified by Q23 and Q24, buffered by Q26 and is sent to the video amplification gain switching circuit of Q27, Q28, Q29 and IC9. The video amplifier gain switching circuit includes a feedback circuit consisting of sample and hold Q30 and dc amplifier IC8 and Q25. IC11 generates clamp pulse from HD pulse and SH3 pulse supplied from the TG-57 board circuit. Output signal from this circuit is sampled at Q30 with the clamp pulse of IC11, amplified by dc amplifier IC8 and Q25, and is fed back to the video amplifier gain switching circuit has an error correction voltage. By using this feedback loop, black level is prevented from fluctuation even video gain switched for 0 dB/9 dB/18 dB.

Gain of video amplifier is determined by the ratio of Rb/Ra. R106/R108/R109 determine Ra value. R112/R113/R114 determine Rb value. Resistance values of Ra and Rb vary in accordance with on/off of Q27/Q28/Q29. On/off switchings of Q27/Q28/Q29 in relation with GAIN switch positions are shown in the following table. Q24 collector receives test SAW signal input for test mode operation and B.BLK.SH signal input for black tracking operation.

| | 0 dB | 9 dB | 18 dB | 24 dB |
|---|---|---|---|---|
| Q27 | OFF | ON | OFF | OFF |
| Q28 | OFF | OFF | ON | ON |
| Q29 | ON | ON | ON | OFF |

**Table 4-1. GAIN Switch**

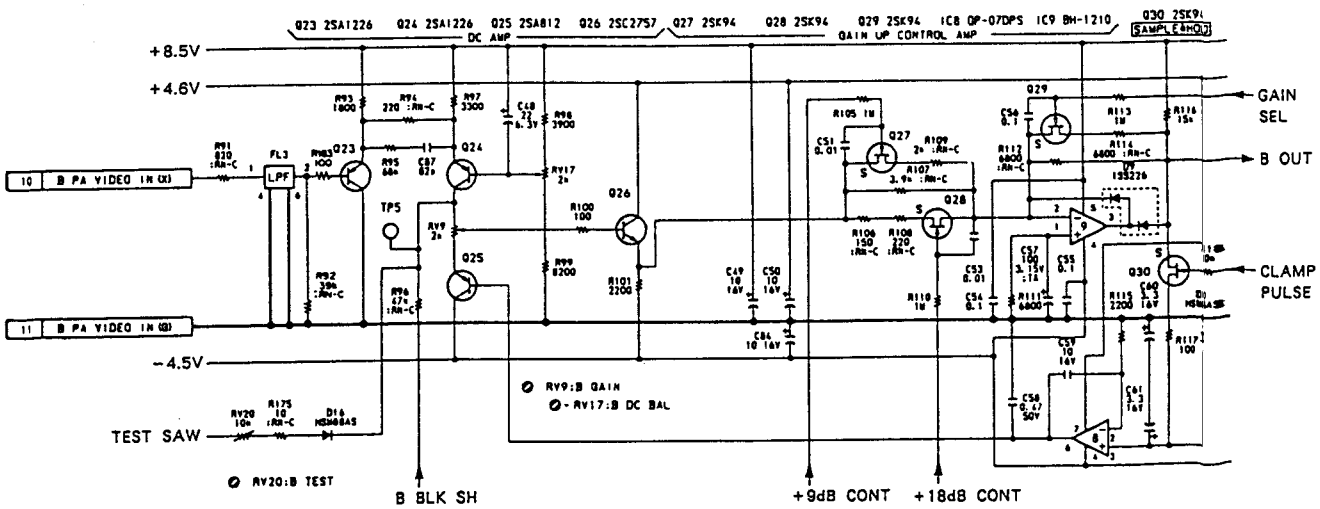



**Fig. 4-1. Video Amplifier Gain Switching Circuit**

## 4-3. BLANKING CLEANING CIRCUIT

This circuit consists of Q31 and Q32.
During horizontal effective period of video signal, Q31 is turned on so that blue channel signal passes through this circuit. During horizontal blanking period, Q31 is tuned off to cut-off the blue channel signal. Q32 is turned on instead so that blanking level is clamped to ground level and blanking period is cleaned.
Control signal for switching these transistors is PRE BLKG pulse supplied from the SG-152 board. IC12 generates inverted phase PRE BLKG pulse that is used for blanking cleaning.

## 4-4. GAIN CONTROL CIRCUIT

Gain control amplifier that operates for white balancing is included in IC10. Blue channel signal is applied to pin 1 of IC10 while blue channel video gain control voltage is applied to its pin 13 with +2.5±2.5 Vdc range from the AT-49A board. With the blue channel gain control dc voltage, gain of the blue channel signal is determined.
Controllable range of auto white balance, when filter-1 is selected, is +500° K for 3200° K. This circuit has also white shading correction function, as white shading correction signal is input to pin 15 of IC10. In order to prevent pedestal level from adverse effect of fluctuation due to white shading correction signal, the dc voltage obtained by RV10 (B-CH V MOD BALANCE) is fed to pin 17 of IC10.

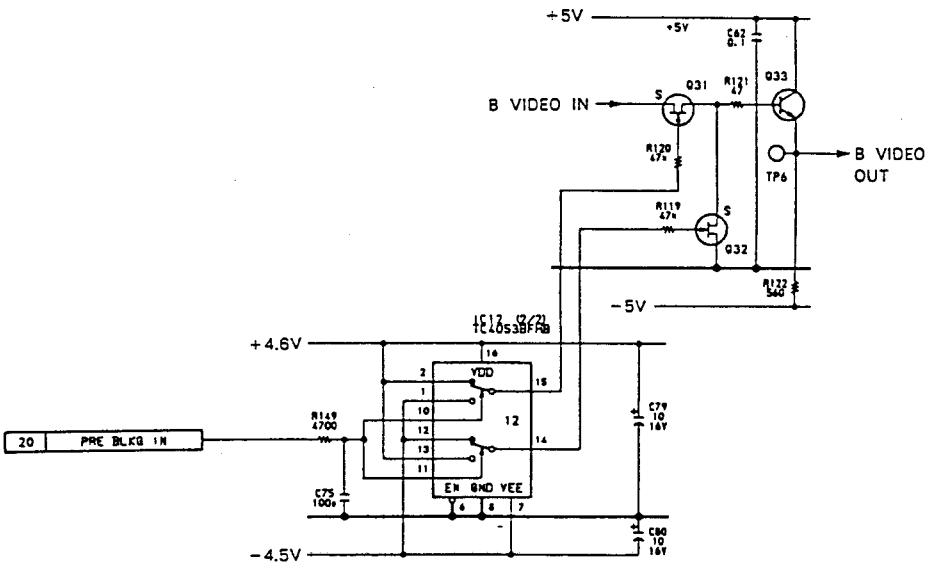



Fig. 4-2. Blanking Cleaning Circuit

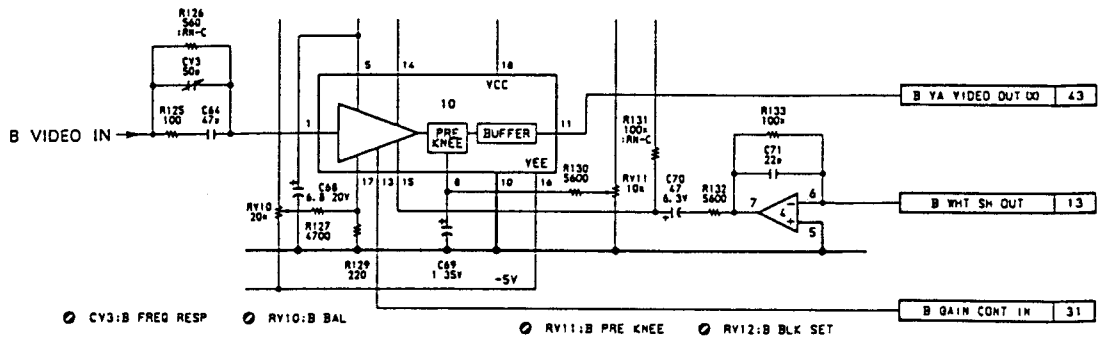



Fig. 4-3. Gain Control Circuit and Pre-knee Correction Circuit

## 4-5. PRE-KNEE CORRECTION CIRCUIT

This circuit is included in IC10. This circuit is non-linear amplifier that performs signal compression for the purpose of widening dynamic range of output signal.
The dc voltage that is obtained by RV11 (B PRE KNEE) is input to pin 8 of IC10 that changes impedance of non-linear amplifier inside pre-knee correction circuit in order to determine the starting point (knee point) of signal compression.

## 4-6. HORIZONTAL SHADING CORRECTION WAVEFORM GENERATOR

This circuit generates positive and negative polarity sawtooth wave signal by IC4 (1/4) and IC6 (1/2) that are housed in hybrid IC (IC15 : BH1252), as triggered by HD signal. When test mode is established by turning on S3 (TEST SAW ON/OFF) switch on the SG-152 board, sawtooth wave generation is prohibited by TEST ENABLE signal supplied from Q4, so that shading correction signal will not be sent to output. Horizontal sawtooth wave of inverted polarity is obtained at IC4 inside IC15. Positive polarity sawtooth signal and negative polarity sawtooth signal are mixed by RV4, RV5, RV6, RV7, RV8 and RV9 and are sent to output. IC4 (3/4, 4/4) inside IC15 is a horizontal parabola wave generator. Positive polarity parabola and negative polarity parabola are mixed by RV10, RV11 and RV12, and are sent to output.

## 4-7. VERTICAL SHADING CORRECTION WAVEFORM GENERATOR

The sample pulse that is input to pin 21 of CN1 is integrated by an integrator circuit including RV14 and is sent to pin 5 of latch IC14 that is housed inside IC15. Thus, the vertical blanking pulse that uses HD signal as its clock, is output from pin 1 of IC14. Vertical blanking pulse width can be adjusted by RV14. IC14 output has two feeds. One output is sent to the positive and negative polarity V. sawtooth wave generators of IC5 (1/2) and IC6 (1/2) located inside IC15, as trigger signal. Positive and negative polarity sawtooth wave is in fact generated by IC5 (1/4) and IC6 (2/2). When test mode is established by turning S3 (TEST SAW ON/OFF) switch on the SG-152 board on, generation of positive/negative V.sawtooth wave is prohibited by the TEST ENABLE signal that is input to IC6.

The other signal is applied to pin 6 of IC1 inside IC15 and selection is mode so that the R, G and B V block shading correction signals are applied to the R, G and B main line signals, respectively.
Inverted polarity vertical sawtooth wave appears at IC5 (1/4) and IC5 (2/4) inside IC15. Positive and negative polarity vertical sawtooth wave signals are mixed by the potentiometers RV13 through RV21 and are output. IC5 (3/4, 4/4) inside IC15 are vertical parabola wave generator circuit. Inverted polarity parabola wave is output from pin 7 and pin 8. Positive and negative parabola waves are mixed by RV22, RV23 and RV24 and are output.

## 4-8. BLACK SHADING CORRECTION WAVEFORM GENERATOR

The mixtured signals of H/V sawtooth wave and H/V parabola wave for R.G.B channels, are sent to pins 14, 4 and 15 of IC2 inside IC15, and are switched on/off at HD rate. The switched signals are buffered by Q1 through Q3 output from pins 47, 53 and 51 of IC15, and are mixed with R.G.B main line video signals at collectors of Q2, Q13 and Q24. When S3 (TEST SAW ON/OFF) switch on the SG-152 board is on, the HD signals that are input to pins 13, 12 and 5 of IC1 inside IC15, are prohibited by the SW signal applied to pin 6 of IC1.

## 4-9. WHITE SHADING CORRECTION WAVEFORM GENERATOR CIRCUIT

The mixtured signals of horizontal sawtooth and vertical sawtooth waves are input to pins 13, 6 and 2 of IC4. The input signals are inverted and amplified by IC4 and are sent to pin 15 of IC13, pin 15 of IC7 and pin 15 of IC10 where they are mixed with R/G/B main line video signals. Vertical sawtooth wave is normally generated through the RV16/RV17/RV18. But when extender is used with lens, the control voltage (EXTENDER ON/OFF signal) is given from lens circuit to flip an analog switch IC3 so that vertical sawtooth wave is generated through the potentiometers RV13/RV14/RV15. Thus the vertical saw shading that extender lens causes, can be compensated.

# SECTION 5
# IE-20A BOARD

## 5-1. OUTLINE OF IMAGE ENHANCER BOARD

IE-20A board consists of following circuits :
- Delayed signal generator
- Sample pulse generator
- AGC circuit
- Horizontal detail signal generator
- Vertical detail signal generator
- Level dependent circuit
- Crispening circuit
- DTL signal output circuit

## 5-2. DELAY SIGNAL GENERATOR

Green channel signal is input to pin 39 of CN1, buffered by Q1 and fed to two circuits. One feed is sent to buffer Q2 while the other is sent to Q3 where the signal is clamped to ground level. The green signal clamped by Q3 is sent to a 28 MHz modulator IC1. 28 MHz carrier signal to be used by an AM modulator IC1, is supplied from pin 9 of CN1, buffered by Q15 and sent to IC1.
The green channel signal is AM modulated by 28 MHz carrier at IC1, and the 28 MHz-AM-modulated-G-signal is buffered by IC2 and sent to delay line DL1 (1/2). The G−signal that is delayed for 1H period by DL1 (1/2) is sent to gain control amplifier consisting of Q4 through Q8. Amplification gain of the gain control amplifier can be determined by dc voltage at pin 7 of IC4 so that it acts as an AGC amplifier. Generation of 2H delayed video signal requires another 1H delay for the already 1H delayed signal that is supplied from the gain control amplifier Q4 through Q8. Output from the gain control amplifier is supplied from Q4 emitter and Q8 emitter with inverted polarity and sent to base of Q9 and Q10. The 1H delayed signal is full-wave rectified at Q9/Q10, and is demodulated by a low-pass filter of C20/L5/CV2. The demodulated G−signal has two output feeds. One output is buffered by Q12 and sent to detail signal generator circuit as the 1H delayed signal. The other output is sent as the main line G−channel output signal to buffer Q13/Q14 and to the PR-132 board.
The 0H non-delayed signal, 1H delayed signal and 2H delayed signal passed through Q2/Q12/Q23 are sent to detail signal generator and AGC circuit.

## 5-3. SAMPLE PULSE GENERATOR

This circuit consists of IC8, IC9 and IC10, having the function of generating a REF pulse (0H sample pulse), AGC sample-and-hold pulse for 1H delay circuit (1H sample pulse), and AGC sample-and-hold pulse for 2H delay circuit (2H sample pulse).

Clock pulse used here, is the sample pulse from the SG-152 board. Since main line video signal is delayed for 1H period, the sample pulse is also delayed for 1H period.

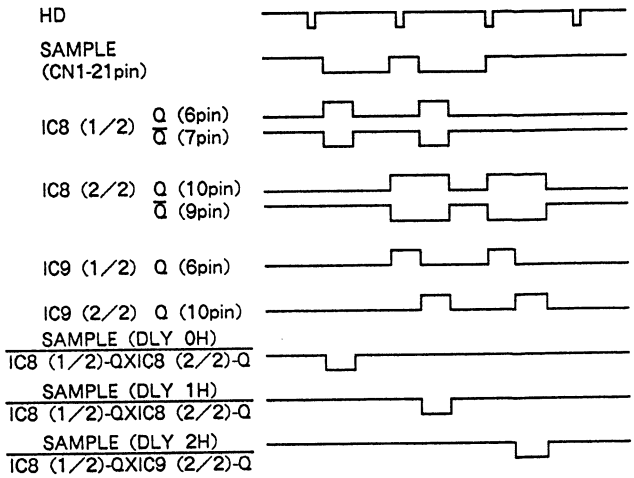



**Fig. 5-2. Sample Pulse Generator Timing Chart**

## 5-4. AGC CIRCUIT

As the 29.5 MHz (1888fH) modulated G−channel signal passes through 1H delay line, it receives attenuation of approximately 20 dB, this circuit provides amplification for the G−signal to compensate for the attenuation.
Gain of the AGC amplifier is controlled by the dc voltage that is generated by the AGC circuit consisting of Q24 through Q30 and IC4.
The control voltage to amplify the 1H delayed signal is generated by Q24/Q28/IC4 (1/2). The 0H non-delayed signal (the G−signal that is input to the IE-20A) is buffered by Q2, clamped to ground signal level with Q27 and is sampled-and-held at Q25 by the 1H sample pulse supplied from inverting amplifier Q32. A reference white pulse has been already inserted and added in the VA-83 board to the position where the 0H signal will be sampled at Q31 and 1H delayed signal will be sampled at Q32.
The sampled and held output from 0H non-delayed signal and the sampled and held output from 1H delayed signal are sent to error amplifier IC4 (1/2) where these two signals are compared to detect error voltage from the level difference between the 0H non-delayed signal and the 1H delayed signal. The detected error voltage is sent back to gate Q6 so that internal resistance of Q6 is changed to control gain of the amplifier. Thus, the AGC circuit operates so that level difference between the 0H non-delayed signal and the 1H delayed signal becomes zero. The AGC circuit for the 2H delayed signal amplification functions in the same manner.

## 5-5. HORIZONTAL DETAIL SIGNAL GENERATOR

This circuit consists of Q34 through Q37, DL2 and IC5. The 0H non-delayed signal, the 1H delayed signal and 2H delayed signal are mixed with ratio of 1 : 2 : 1 with R79/R80/R81 and are input to base of Q34. The horizontal detail signal generator circuit is to emphasize the detail of signal centering around 4 MHz. If subcarrier frequency component is included in a object of shot picture, that portion of picture will show beat signal on monitor screen. In order to prevent beat, subcarrier frequency component should be removed from the signal.

Subcarrier signal phase is in phase with 0H non-delayed signal and 2H delayed signal, and is in opposite phase with 1H delayed signal. Therefore, by mixing the 0H, 1H and 2H delayed signals with ratio of 1 : 2 : 1, they are canceled each other as shown in Fig. 5-3, the subcarrier component is removed. To generate detail signal from R−channel signal, R−channel signal is mixed at base of Q34.

The signal that is amplified by Q34/Q35/Q36 is divided into two outputs. One output signal is delayed by DL2 for 120nsec, buffered by Q37 and sent to pin 2 of IC5 (inverting input pin). The other output signal is passed through a low pass filter of LV1/C57 and input to pin 1 of IC5 (non-inverting input pin).

Horizontal detail signal is supplied from pin 3 of IC5 and is mixed with vertical detail signal by RV7.

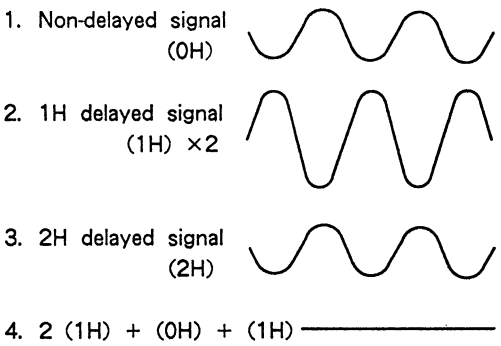



**Fig. 5-3. Subcarrier Removal**

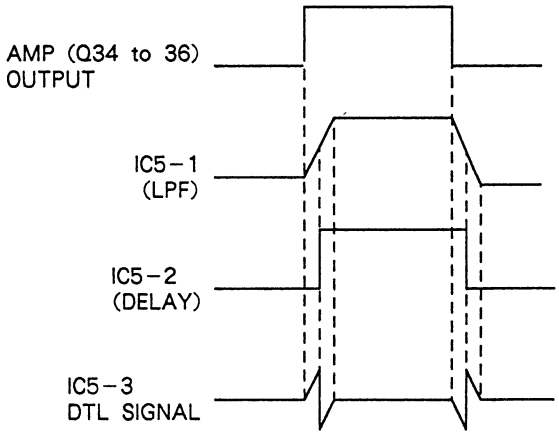



**Fig. 5-4. Horizontal Detail Signal Waveform**

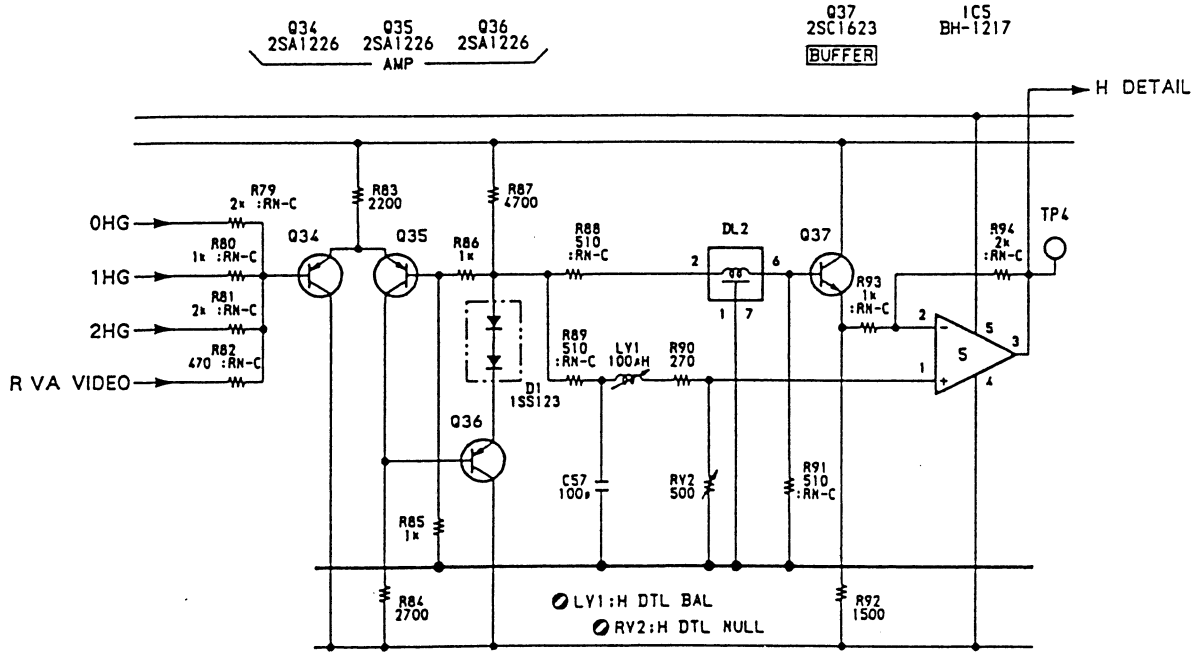



**Fig. 5-5. Horizontal Detail Signal Generator**

## 5-6. VERTICAL DETAIL SIGNAL GENERATOR

Vertical detail signal is generated by first adding the 0H non-delayed signal and the 2H delayed signal, and then subtract the two times multiplied 1H delayed signal from the added output.
Q48 and Q49 constitute differential amplifier. The 0H non-delayed signal and 2H delayed signal are input to base of Q48 while the two times multiplied 1H delayed signal is input to base of Q49. The two times multiplied 1H delayed signal is phase-inverted by Q49 so that the (0H+2H) −2 (1H) signal as a vertical detail signal is supplied from the differential amplifier. The vertical detail signal is band-width limited by the low-pass filter (L7, C72) for 1 MHz/−3 dB, buffered by Q50 and is mixed with horizontal detail signal with RV7.

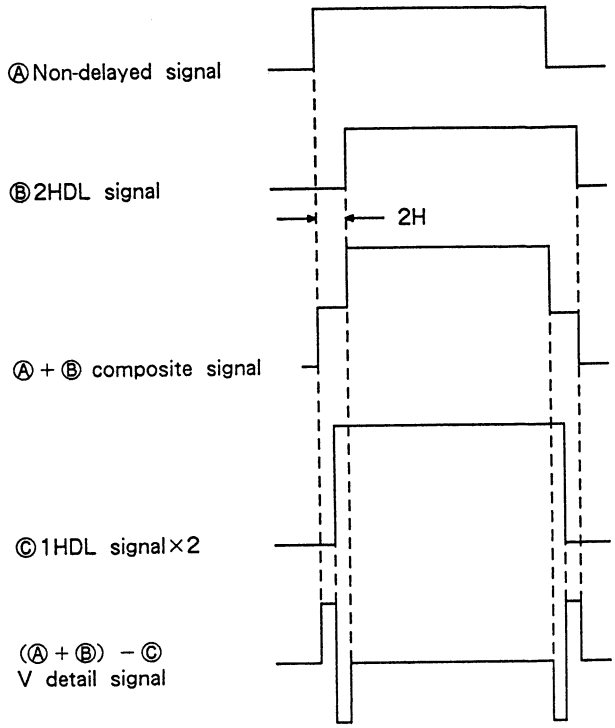



Fig. 5-6. Vertical Detail Signal Waveform

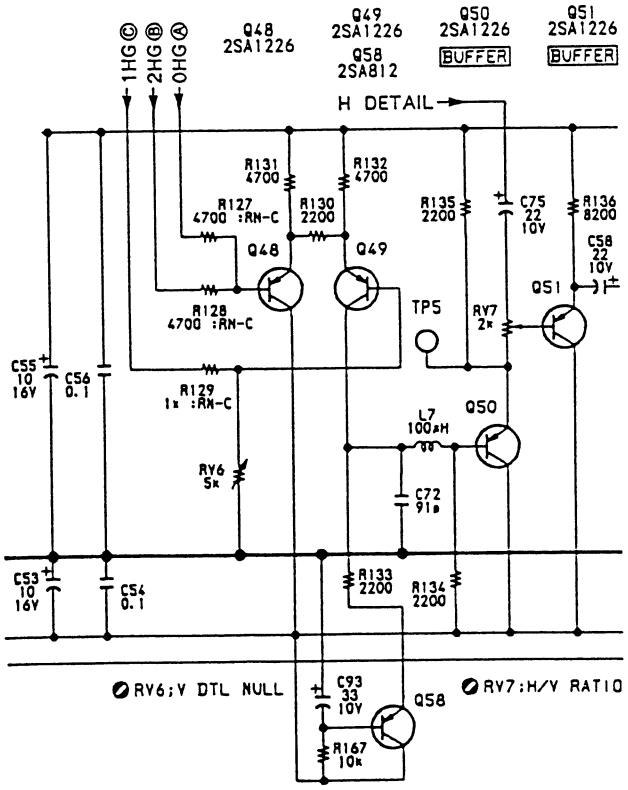



Fig. 5-7. Vertical Detail Signal Generator

## 5-7. LEVEL DEPENDENT CIRCUIT

Video signal amplitude changes in accordance with a object. When video signal has low amplitude (when the object has low brightness), the noise component that accompanies with detail signal becomes significant, resulting in deterioration of S/N ratio in the darker area of picture. In order to prevent this phenomenon, detail signal is turned off where video signal has low amplitude level.

Level dependent circuit consists of Q52, Q53, Q54 and Q38. The 1H signal is clamped to ground level by Q52 and input to differential amplifier of Q53/Q54. Since operating point of Q54 is determined by RV8, operating point of level dependent circuit is adjusted by RV8.

Output of differential amplifier Q53/Q54 is sent to gate of Q38 where impedance between source/drain terminals of Q38 is changed so that detail signal is muted depending upon amplitude of video signal level.

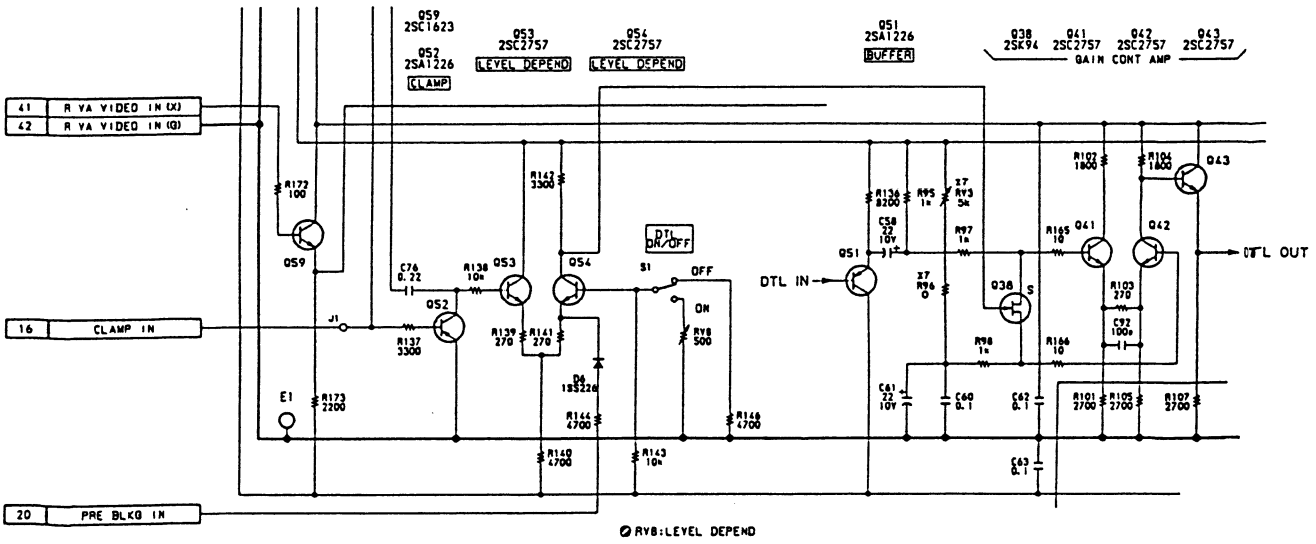



Fig. 5-8. Level Dependent Circuit

## 5-8. CRISPENING CIRCUIT

The crispening circuit removes low amplitude noise from the DTL signal. The DTL signal is sent to the gain control amplifier.

As shown in Fig. 5-9, the DTL signal is sent to diodes D4 and D5. When the DTL signal amplitude exceeds a voltage difference between anode and cathode approximately 0.3V, the diode is turned on and the DTL signal is sent to the output. The DTL signal and noise components of less than 0.3V amplitude are thus grounded and removed. This crispening level (voltage difference between D4 anode and D5 cathode) can be adjusted by RV4 so the amplitude of the DTL small signal (mainly noise component) to be removed can be adjusted by RV4. When gain is manipulated, Q56 (+9 dB) and Q57 (+18 dB) are turned on to increase the crispening level to remove noise.

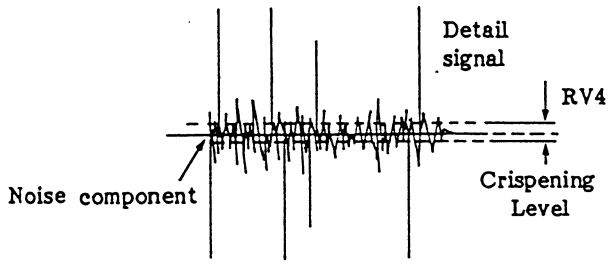



Fig. 5-9. Crispening Signal Waveform

## 5-9. DTL SIGNAL OUTPUT CIRCUIT

The amplitude of the DTL signal from the crispening circuit is adjusted by RV5 and sent to pin 4 of IC7. The input DTL signal is amplified by 6 dB and sent from pin 6 of IC7 to the PR-132 board via buffer Q47. To block the DTL signal from the main line video signal during auto black balance and auto white balance operations, the BLK EN and WHITE EN signals are supplied from the AT-49A board to pin 8 of IC7. When the BLK EN signal or WHITE EN signal reaches level "L", the DTL signal output from IC7 is inhibited.

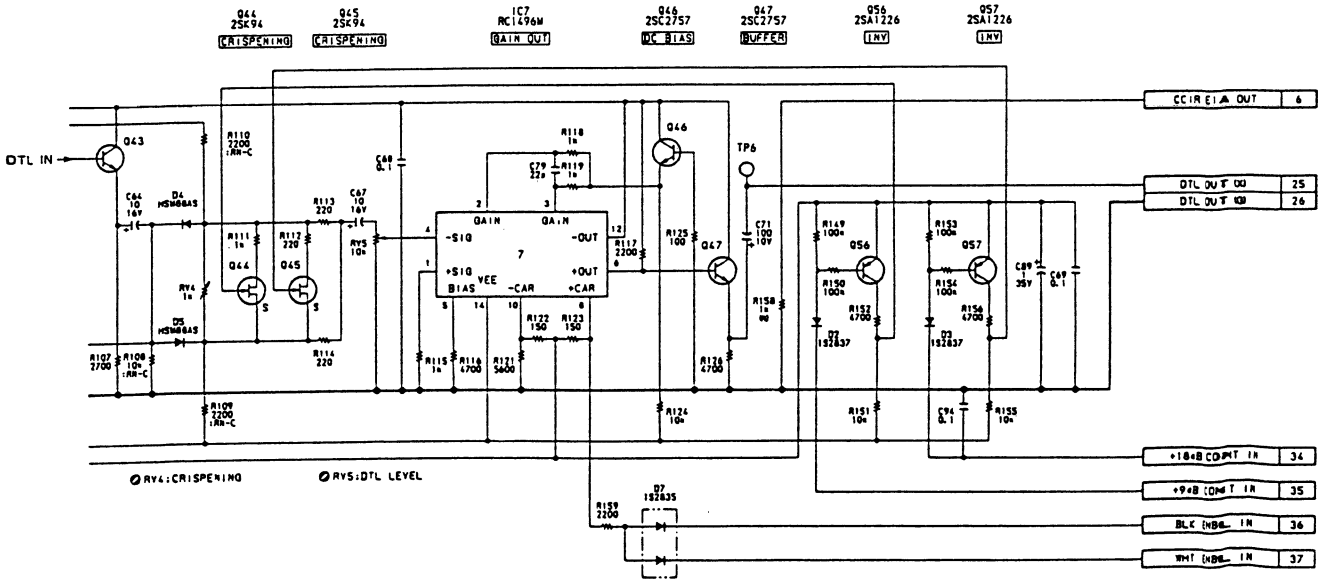



Fig. 5-10. Crispening Circuit and DTL Signal Output Circuits

# SECTION 6
# PR-132 BOARD

## 6-1. OUTLINE OF PR-132 BOARD

The PR-132 board receives input video signals of R and B signals from the VA-83 board and G signal from the IE-20A board. R.G.B input signals receive the signal processing in the following circuits and then sent to the EN-79 board.

- Flare compensation and pedestal control
- Masking circuit
- Knee correction
- DCC (dynamic contrast control) circuit
- Gamma correction
- White clip circuit

## 6-2. FLARE COMPENSATION AND PEDESTAL CONTROL CIRCUIT

Flare is the name of phenomenon that a part of incident light which has fallen into CCD photo-sensor, is reflected by photo-sensor so that the reflected light is again reflected by optical system (including lens) and falls into photo-sensor again.
Amount of flare increases in proportion to the amount of incoming light. When amount of reflected light (flare) increases, pedestal level increases and contrast of video level decreases.

Since amount of pedestal level increase (amount of flare) is proportional to the mean value of the amount of incident light, flare compensation circuit detects a input primary color signal at the average value and finds the average picture level (APL) for the DC. A component proportional to the APL is added to the primary color signal after its phase is inverted. The G signal supplied from pin 3 of IC6, is input to pin 4 of IC3 as main line video signal and is fed back via RV11 and R68. The feed-back signal is average-level rectified by R67/C26 to be converted to dc voltage and input to pin 2 of IC7. Since reference dc voltage is applied to pin 3 of IC7, comparison voltage is output from pin 1 of IC7. Output voltage is input to pin 6 (inverting input terminal) of IC7. The G signal from pin 3 of IC6 is also sent to Q19 where its blanking period is sampled by clamp pulse, rectified by C25 and input to pin 5 (inverting input terminal) of IC7. The input voltages at pins 6 and 5 of IC7 are compared so that comparison output voltage is fed back to IC6 so that pedestal level can be controlled. Since output voltage for flare compensation is in reversed phase with APL of input signal, amount of input video level due to flare effect is deducted by this feed-back. In order to control pedestal level from external equipment, the external control voltage is input to pin 6 of IC7 through resistor R64.

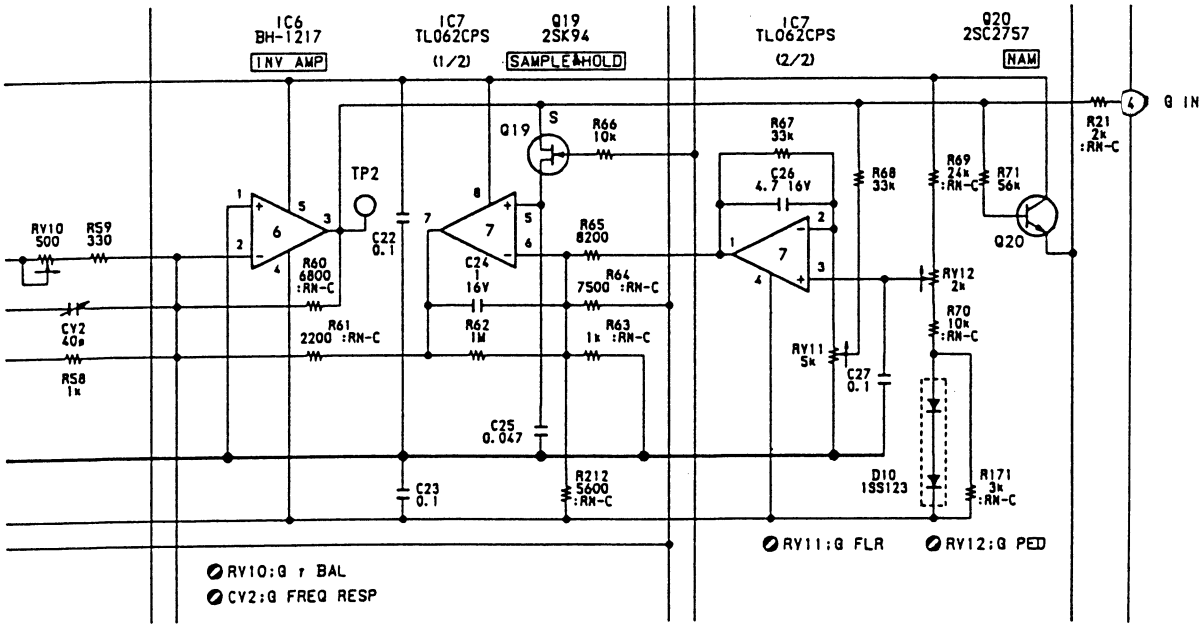



Fig. 6-1. Flare Compensation and Pedestal Control Circuits

## 6-3. MASKING CIRCUIT

Masking circuit consists of Q48 through Q74. It adds very small amount of primary signal of other colors to respective R.G.B signal outputs to correct color reproduction of CCD unit.
S4 (MASKING ON/OFF) is used whether masking signal output is added to R.G.B respective signal or not. Even through S4 is turned on or off, white balance is not affected.
When masking input signals are named as R, G and B, and masking output signals as R', G' and B', output signals can be expressed by the following equations. Matrix constants (a, b, c, d) can be determined by RV29, RV30, RV34 and RV35.

$$R' = a\,(R-G)$$
$$G' = b\,(G-R) + c\,(G-B)$$
$$B' = d\,(B-G)$$

These potentiometers are set in accordance with color reproductive characteristics based on the EBU standard at the factory shippment, therefore, S4 (MASKING ON/OFF) is set to OFF position.

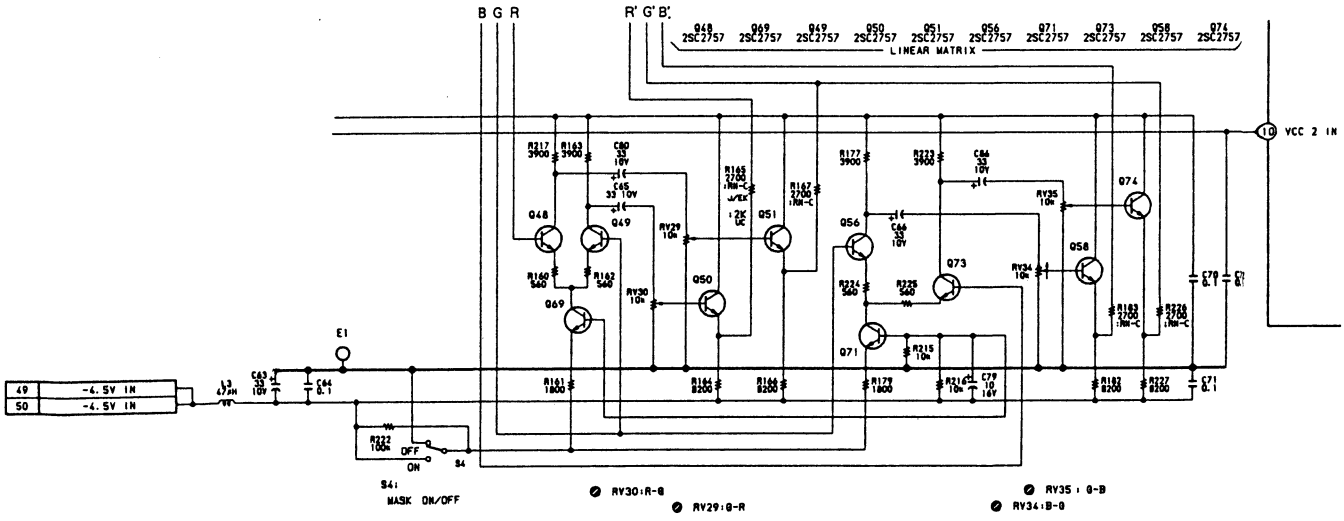



Fig. 6-2. Masking Circuit

## 6-4. KNEE (Dynamic Contrast Control) CORRECTION CIRCUIT

IC3 (BH1251) is a hybrid IC which contains the knee correction and white clip circuits. The knee correction circuit makes the dynamic range of the camera signal wider when an object with high intense illumination is viewed. Optimum contrast is still maintained.

### 6-4-1. Knee Correction Circuit

The red signal knee correction circuit consists of internal IC1, D1 and RV3 in the hybrid IC3 (Fig. 6-3). The green signal knee correction circuit consists of internal IC2, D5 and RV7. The blue signal knee correction circuit consists of internal IC2, D6 and RV12. These knee correction circuits compress the respective signals in accordance with the knee curve. Fig. 6-3 shows the equivalent circuit of the knee correction circuit. The starting point (knee point) of signal compression is determined by the voltage at point-B as shown in Fig. 6-3. The compression ratio (knee slope) of the signal is calculated from the following equation. Signal compression waveforms are shown in Fig. 6-4.

$$\frac{r+r'}{R+(r+r')}$$

Since the red, the same way green and blue knee correction circuits operate only the green signal knee correction circuit is explained.
When dc voltage is applied to pin 6 of IC2, diode D5 is put into conduction by the dc voltage supplied from IC2, thus determining the starting (knee point) level of peak signal compression.
When the dynamic contrast control (DCC) switch is set to the ON position, controlling dc voltage level applied to pin 6 of IC2, is changed in proportion to the input green signal amplitude so the knee point (signal compression starting point) is changed in proportion to the input green signal amplitude. When the DCC switch is set to OFF, the fixed dc voltage is generated by RV9 with analog switch IC3, is applied to pin 6 of IC2 to determine the knee point. Knee slope of the green signal is adjusted by RV7.

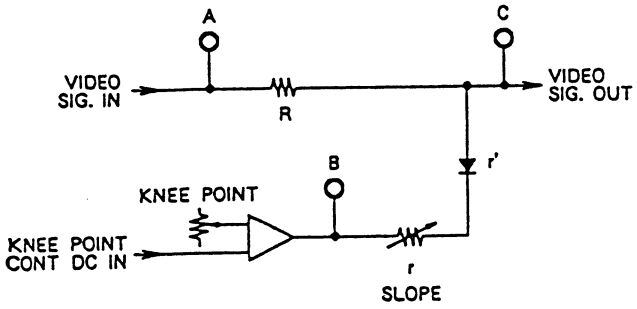



Fig. 6-3. Equivalent Circuit

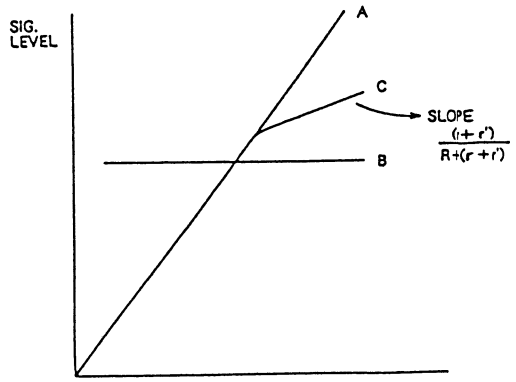



Fig. 6-4. Signal Compression Waveforms

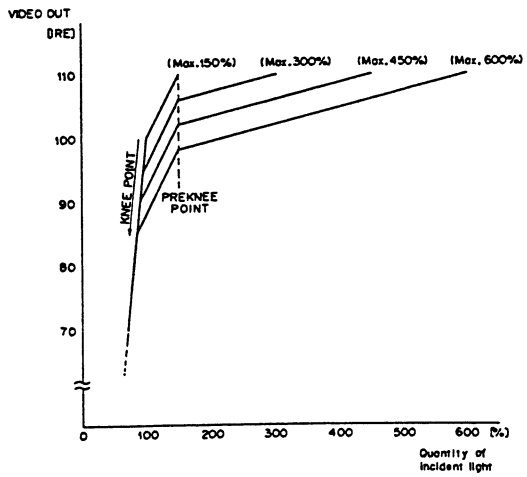



Fig. 6-5. Knee Characteristics

### 6-4-2. DCC Circuit (Dynamic Contrast Control)

The NAM circuit consists of Q1, Q7, Q16 and Q15 in hybrid IC3 (BH1251). The red signal is input to the base of Q1, the green signal to the base of Q7 and the blue signal to the base of Q16. The dc voltage is determined by RV8 and sent to the base of Q15. Therefore, in this NAM circuit, the signal with the highest amplitude of the red, green, blue signals and the dc voltage is output from the NAM circuit. The output of the NAM circuit is buffered by Q8, peak-rectified using D4 and C7, and converted to dc voltage which controls the knee point. As long as the R/G/B signal amplitude is lower than the dc voltage level determined by RV8, the knee point is made constant by the RV8 dc voltage. When any red, green or blue signal attains higher signal level than the RV8 dc voltage level, the output of the NAM circuit is changed to make the knee point lower than the constant knee level. Thus RV8 determines the starting point of the DCC operation.

The dynamic contrast control (DCC) circuit operates when the input signal whose white peak is higher than the white clipping level, is introduced from the CCD imager. As long as the input signal amplitude remains lower than the white clipping level, the knee point will have no effect on the output signal. Therefore the output video signal maintains linear photo-electric characteristics from pedestal to white clipping level. When incident light brighter than the white clip level is introduced to the CCD imager, the knee point is pulled to a lower level and the signal is simultaneously compressed. An object which is brighter than the white clip level can also be reproduced in the output video signal. To obtain correct white balancing, the knee circuit and the white clip circuits are turned temporarily OFF during auto white balancing. The DCC circuit is temporarily made an open loop. Because of this circuit operation, there is a chance that the signal level decreases at the moment when auto white balance is completed and the DCC circuit returns to a closed loop. In order to prevent this decrease of signal, a limiter circuit of Q9 and RV4 is provided to control the signal peak of the NAM circuit output. The NAM circuit output signal peak-rectified by D4 and C7, is sent to pin 5 of dc amplifier IC1. The dc amplifier IC1 determines to what extent the knee point should be lowered with respect to the input dc voltage. Gain of the dc amplifier is determined by RV5.

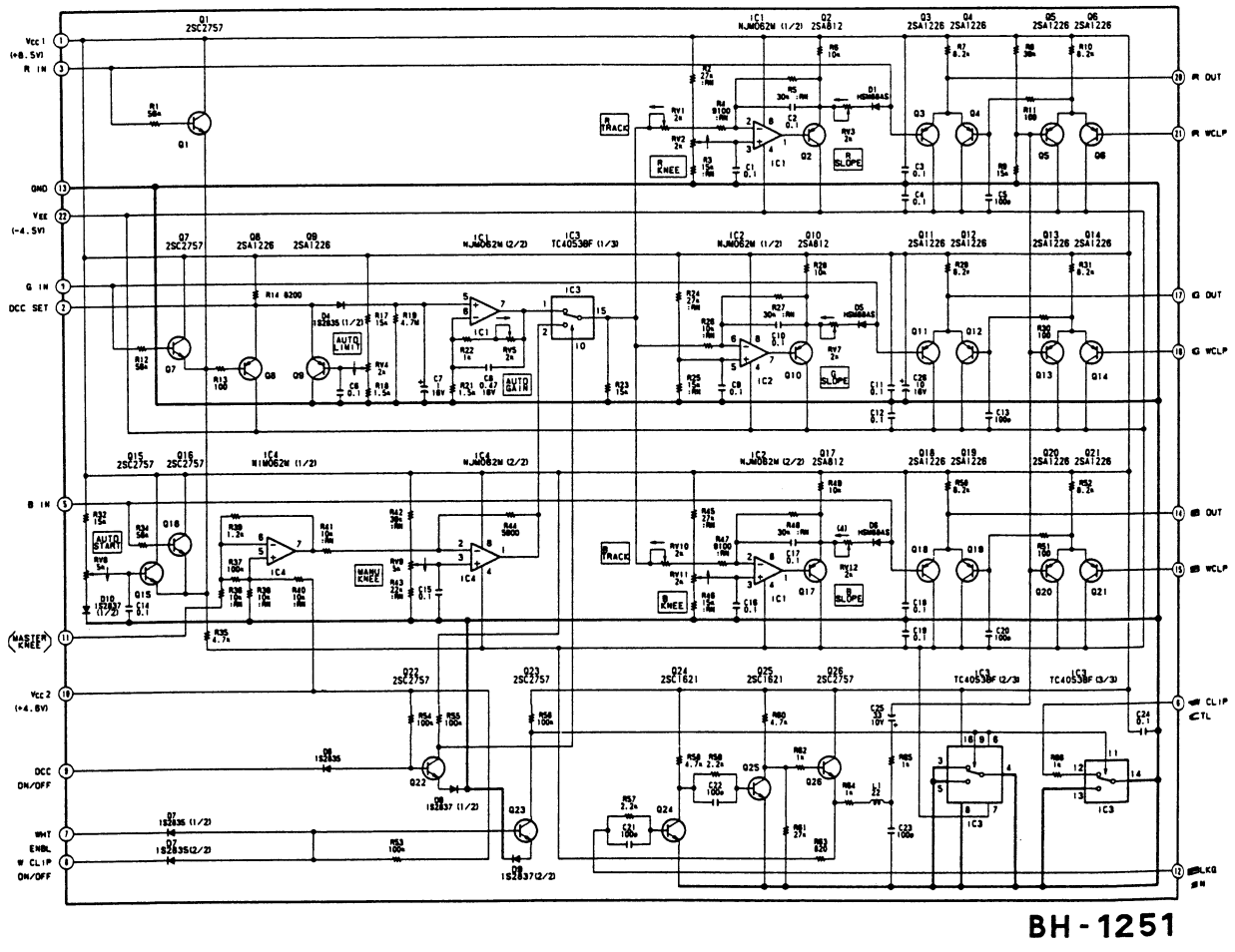



Fig. 6-6. DCC Circuit

## 6-5. WHITE CLIP CIRCUIT

The white clip circuit for the red signal consists of Q3 through Q6 in hybrid IC3 (BH1251), which holds the red signal peak at 750 mV. The signal blanking is also contained in this circuit.
When the blanking pulse is high (during the video signal period), RV7 voltage is input. If the red signal becomes higher than the RV7 dc voltage, the red signal peak is clipped. When the blanking pulse becomes low (blanking period), the DC voltage becomes lower than the black level of the red signal, and blanking is added. When switch S5 is set to OFF, or the WHT EN (white enable) signal is set low, the clip level is raised so white clip operation is disabled. Switch S5 should only be used during adjustment, and is normally set to the ON position. In order to obtain the white balancing, the WHT EN signal becomes low during auto white balance and disables the white clip and knee correction.

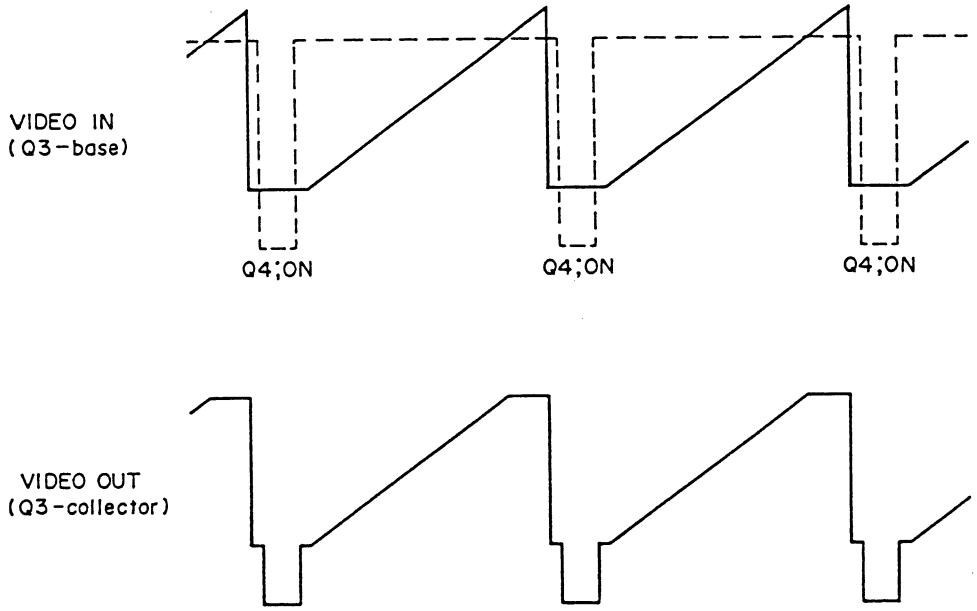



**Fig. 6-7. White Clip Waveforms**

## 6-6. GAMMA CORRECTION CIRCUIT

The red signal from the white clip circuit is sent to the gamma correction circuit consisting of Q10 through Q13, D5 and D6.
The red signal is amplified by Q10, buffered by Q12 and sent to the gamma signal generator circuit consisting of Q11, D5 and D6. Utilizing the square characteristics of a diode, Q11 generates the gamma correction signal. The gamma correction signal is passed through switch S1 and mixed with the red signal through RV8. By varying the mixing ratio, the amount of gamma correction can be adjusted. Addition or non-addition of the gamma correction signal is determined by switch S1.
The red signal from the gamma correction circuit is amplified by IC4 and is sent to the EN-79 board from pin 29 of CN1. Feed-back clamp is provided by Q14 and IC14. The red signal is clamped by the SAMPLE DLY 0H pulse so the red signal is clamped to 0V.

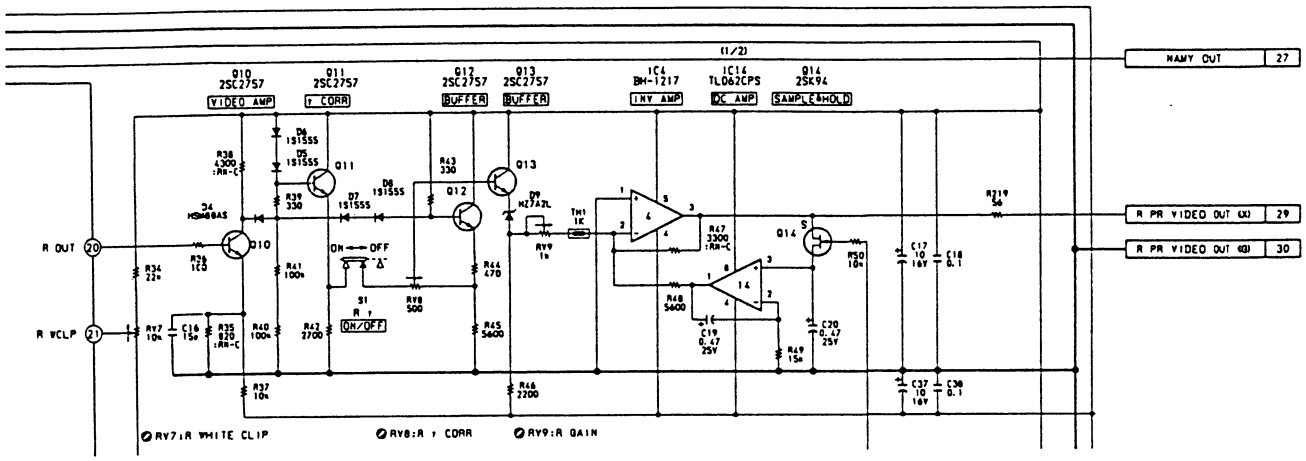



Fig. 6-8. Gamma Correction Circuit and Output Circuit

# SECTION 7
# EN-79 BOARD

## 7-1. OUTLINE

The EN-79 board consists of the following circuits to generate composite video ( VBS ) signal and component signals (Y, R−Y, B−Y) for the Betacam from the R, G and B signals.

- CAM/BAR selector
- Color bar generator
- Y−matrix
- R−Y/B−Y matrix
- Chroma encoder
- Monitor waveform select switch
- Power save
- Zebra signal mixer

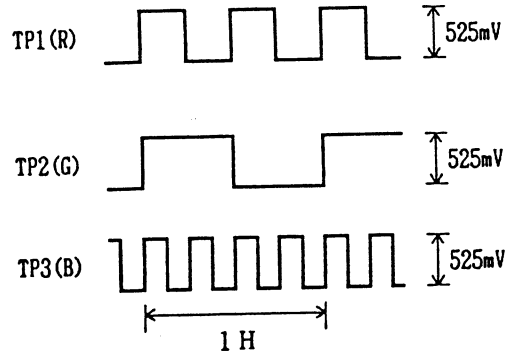



Fig. 7-1. R/G/B Output Signal Waveform

## 7-2. CAM/BAR SELECTOR AND COLOR BAR GENERATOR

IC1 selects the camera signal or the color bar signal. When OUTPUT/DCC select switch is BARS/OFF position, the BARS EN signal goes to a "Low" level to output the color bar signal from IC1. The color bar signal from IC1 is buffered by Q1 through Q3 and sent to matrix circuits. TP1 (R), TP2 (G) and TP3 (B) will have the respective color bar signal waveforms that are generated by IC6 (CX7968A) shown in Fig. 7-1. When the BARS EN signal goes "Low", the color bar signal is generated by IC2 from the BLKG, HD and BAR CK (approximately 3.6 MHz) signals as shown in Fig. 7-2.

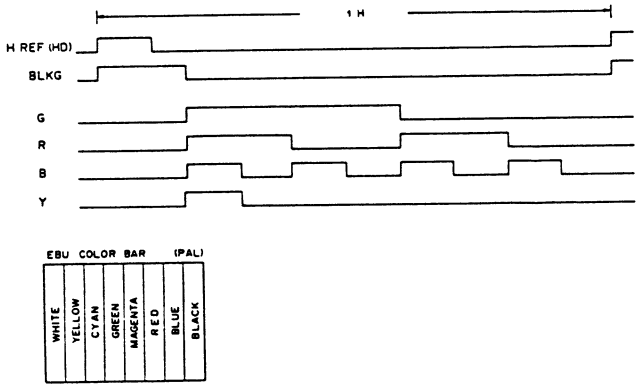



Fig. 7-2. Color Bar Output Signal Timing and Waveform

## 7-3. Y-MATRIX CIRCUIT

The RB1 is a resistor network for Y-matrix and mixes the R, G and B signals with mixing ratio of "Y=0.3R+0.59G+0.11B". This Y-signal is added to the sync signal by RV6, and setup is added to the Y-signal by RV4. When color bar output is selected, 100% white pulse is generated by the color bar generator IC2, added by RV5 and the color bar setup signal is added via R31 and R32, too.
The processed Y-signal is sent to pin 2 of inverter IC3 that has the feedback clamp function. The burst flag (BF) pulse is used as a clamp pulse. The Y-signal from pin 4 of IC3 is inverted by the inverter IC4 (1/2) and sent to the AFM-6 board as Betacam component Y-signal. The Y-signal is delayed by DL1 (338 nsec) to match its phase with that of the chroma signal, buffered by Q14 and Q15 and sent to IC7.
IC7 mixes Y-signal with chroma signal to generate the VBS signal. Y-signal level is adjusted by RV11, Y-signal frequency response is adjusted by CV1 and chroma level is adjusted by RV12. The VBS signal from IC7 is sent to the BNC connector to be supplied to output equipment.

## 7-4. R-Y/B-Y MATRIX AND CHROMA ENCODER CIRCUITS

The R-Y matrix circuit consists of IC10, R60 and RB2. The B-Y matrix circuit consists of IC10, R90 and RB3. The R-Y and B-Y signals are buffered by Q31 and Q32, and sent to the VDA-11 board as Betacam component signals. The R-Y and B-Y signals are used as chroma signal in this equipment. The R-Y signal level and B-Y signal level can be adjusted by RV20 and RV21 respectively.
The R-Y signal is passed through Q10, S1, low-pass filter (consisting of L5, C27, C28), Q11, Q35, Q12 and clamped by BF clamp pulse with Q13. The R-Y signal is then sent to pin 1 of encoder IC8.
The B-Y signal is passed through Q18, S2, low-pass filter (L6, C39, C40), Q19, Q20, Q36, clamped by BF clamp pulse with Q21. The B-Y signal is sent to pin 4 of encoder IC8. The switches S1 and S2 are ON/OFF switches for R-Y axis and B-Y axis to be used during encoder adjustment. The low-pass filters for R-Y signal and B-Y signal are the 1.5 MHz low-pass filters.
The BF pulse is added to the video signal in IC3. The BF pulse is also supplied to the BURST SET circuit consisting of IC9 and D2, where a pulse width is adjusted by RV13. Therefore, a start point of the burst signal is determined. After that, the BF pulse level is adjusted by RV15 to adjust the level of the BURST signal. The chroma signal that is encoded by IC8 is limited its frequency band-width by band-pass filter (FL3). The chroma signal is buffered by Q25, its amplitude is adjusted by RV12 and is mixed with Y-signal.

## 7-5. MONITOR WAVEFORM SELECT SWITCH

The monitor waveform select switch S3 selects the VBS signal output or the G-channel signal to be sent to the output circuit through the BNC connector. When S3 is G position, the G signal with burst, sync and setup is output from the BNC connector. In order to prevent operation error, the MONITOR ENABLE signal is sent to CPU on the AT-49A board through pin 46 of CN1. When S3 is G position, the MONITOR ENABLE signal goes "Low" and the "MONITOR MODE" is displayed in the viewfinder.

## 7-6. POWER SAVE CIRCUIT

When the VBS signal from BNC connectors on the right side panel and rear panel is not used, power in the VBS output circuit and chroma encoder in the EN-79 board is turned OFF, in order to save power. The BNC connectors are located on the right side panel and rear panel.
When VBS OUT connector has no connection, the internal switch in the VBS connector is turned ON. Therefore the approximately 2.8 Vdc bias voltage obtained by divider R138 and R29 on the EN-79 board is supplied to the base of Q4 on the MB-173A board. It raises the emitter voltage of Q4 to +4.6 Vdc to turn Q4 OFF. It sets Q30 OFF and Q34 ON that turns +8.5V power line OFF by Q26, +4.6V power line OFF by Q27 and −4.6V power line OFF by Q29. When the BNC connector is connected to the VBS OUT connector, internal switch in the VBS connector is turned OFF and bias voltage at base of Q3 reaches higher than the collector voltage (+4.6V). Q4 is then turned ON and the power save mode is released. Also, when the video and audio signals are output through a microwave link for on-air application, and a playback adaptor is connected, the power save circuit is automatically cancelled. The power save mode is turned ON/OFF by the EN SAVE 2 signal from the VP-24 board. When the playback adaptor is connected, the EN SAVE 2 signal goes "Low" that ceases encoder power save mode. In the VTR playback mode, in the camera system, the sub-regulator circuit of the SG-152 board is turned OFF, the power is turned OFF except the almost SG-152 board and part of the CCD block. So that save power. Also when playback adaptor is connected, termination of VBS OUT connector is not needed.

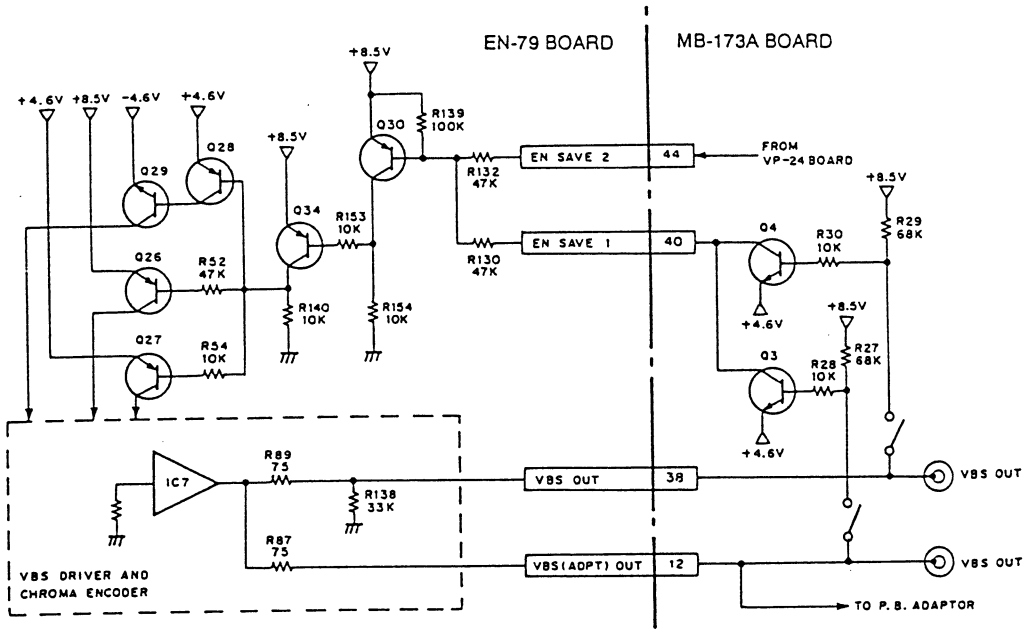



**Fig. 7-3. Power Save Circuit**

## 7-7. ZEBRA SIGNAL MIXING CIRCUIT

The VF signal is the Y−signal from the Y−matrix circuit. The zebra signal is mixed with the Y−signal and sent to the viewfinder.
When the viewfinder ZEBRA ON/OFF switch is ON, the ZEBRA ON/OFF signal goes "Low" and Q4 and Q5 are turned ON and then dc bias voltage is applied to pin 6 of IC5. When dc bias voltage is applied, window comparator IC5 starts detecting the Y−signal amplitude whether or not the the zebra signal should be added.
The Y−signal level of approximately 490 mV is the reference level to add the zebra signal. This zebra signal level is adjusted by RV17.

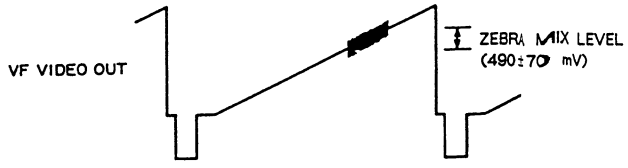



**Fig. 7-4. Zebra Signal Mixing Waveform**

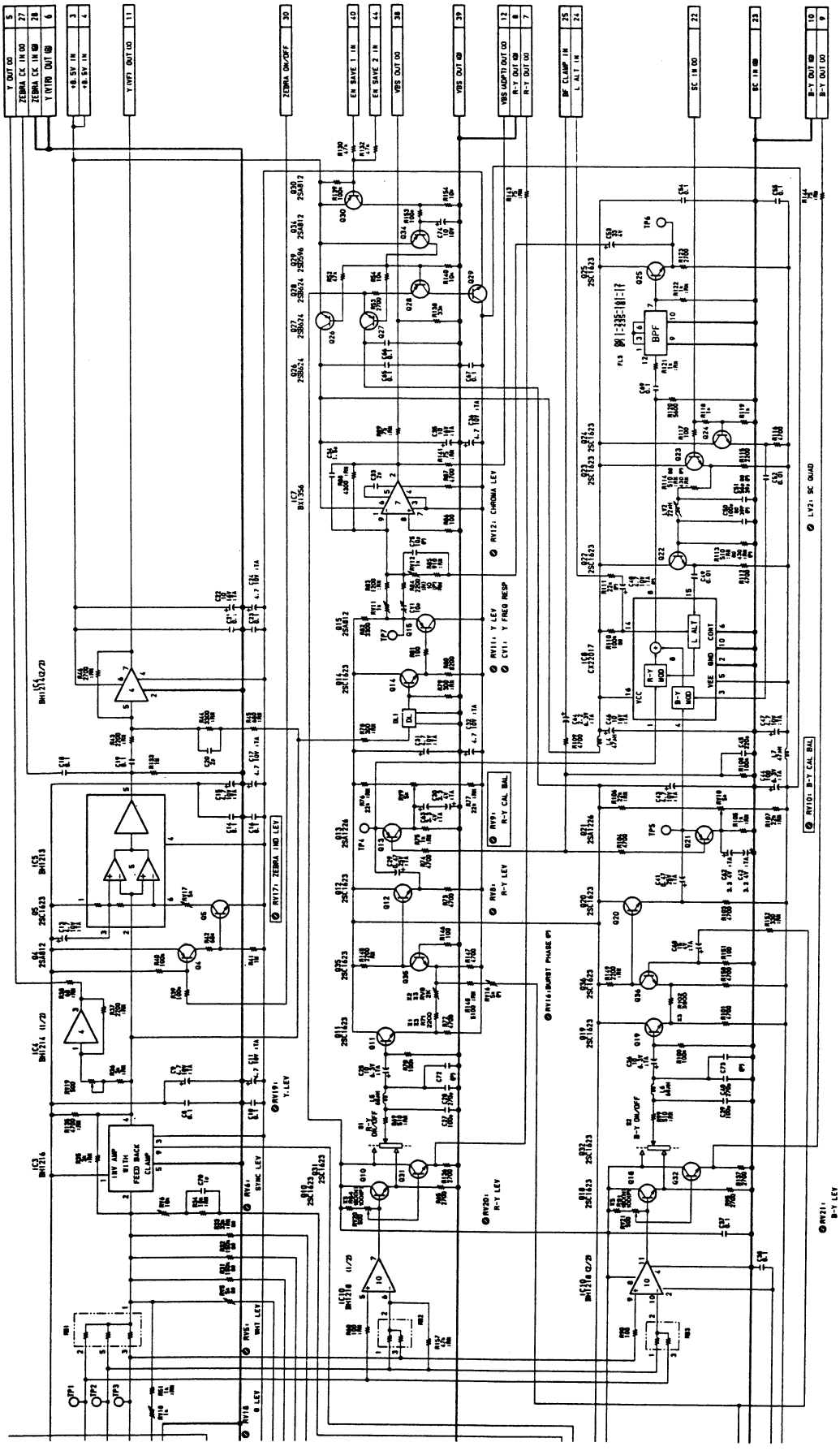


Fig. 7-5.

# SECTION 8
# AT-49A BOARD

## 8-1. OUTLINE

The AT-49A board consists of the following circuits :

- Auto white balance
- Auto black balance
- Filter position detector
- Residual tape display
- Audio CH-1 record level display
- Character generator
- Self-diagnostic

The AT-49A board employs a microprocessor for automatic control of the camera (e.g. as auto white balance and auto black balance). Switch data such as GAIN switch data, TEST switch data or filter position data are taken into the microprocessor and used for optimum automatic control of the camera. The AT-49A board includes other functions such as interfacing with the remote control unit (RM-P3), display of various character/letters on the viewfinder, and self-diagnostics. All these controls in the camera block are performed by the CMOS 8-bit single chip microprocessor IC14 (HD63P05YO). Microprocessor IC14 also has a built-in 8K byte ROM. It has the following features :

- RAM (256 byte)
- I/O port (32 lines)
- Input port (7 lines)
- Output port (16 lines)
- Timer (two types)
- Serial interface circuit
- Interrupt : external port (2 lines), timer (2 lines), serial (1 line), soft (1 line)
- Minimum instruction time : 1 $\mu$ sec

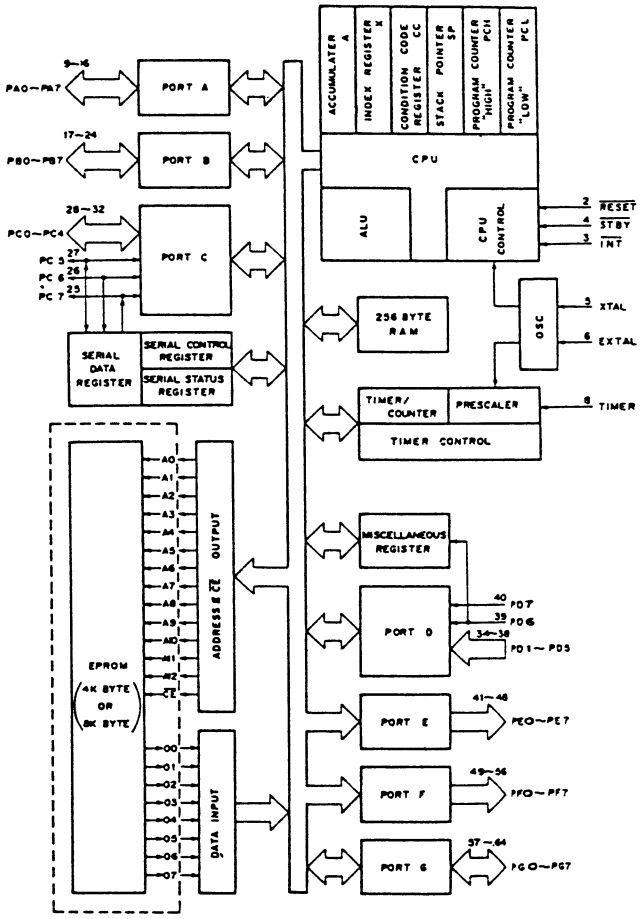



Fig. 8-1. IC14 Block Diagram

| Pin No. | NAME | I/O | FUNCTION | CONNECTION |
|---|---|---|---|---|
| 1 | Vss | I | GND | GND |
| 2 | $\overline{\text{RESET}}$ | I | Resets when power is turned on. | To pin 8 of IC8. |
| 3 | INT | I | Interrupt input port. Enables external S/D input. | To TP2 from the Q4 connector. |
| 4 | $\overline{\text{STBY}}$ | I | Used for putting the MCU in standby mode. | From +4.6V power supply line. |
| 5<br>6 | XTAL<br>EXTAL | I<br>I | Input to built-in clock circuit. Obtains 1 MHz clock from the 4 MHz crystal oscillator. | To crystal oscillator X1. |
| 7 | GND | I | GND | GND |
| 8 | TIMER | I | External input pin for controlling the internal timer circuit. | From CN1 pin 19. |
| 9 | PA7 | I/O | Provides monitor ENBL in. Low for monitoring. | From CN1 pin 4. |
| 10 | PA6 | I/O | Provides shutter SEL in. Not used. | To CN1 pin 9. |
| 11 | PA5 | I/O | Determines whether white balance data is stored for each filter. High for each filter storage. | From S1 (FP INH). |
| 12 | PA4 | I/O | Provides DCC ON/OFF input. Low for DCC on. | To CN1 pin 33. |
| 13 | PA3 | I/O | Provides test EN in/out. Low for test mode. | To CN1 pin 47. |
| 14 | PA2 | I/O | Provides bars EN in/out. Low for active. | To CN1 pin 43. |
| 15 | PA1 | I/O | Provides +9V dB CONT in. Low for active. | To CN1 pin 29. |
| 16 | PA0 | I/O | Provides +18V dB CONT in. Low for active. | To CN1 pin 28. |
| 17 | PB7 | I/O | SHT B5. Not used. | To CN1 pin 12. |
| 18 | PB6 | I/O | SHT B6. Not used. | To CN1 pin 11. |
| 19 | PB5 | I/O | SHT B7. Not used. | To CN1 pin 10. |
| 20 | PB4 | I/O | SHT TAPE. Not used. | To CN1 pin 8. |
| 21 | PB3 | I/O | Provides white BAL preset in. Low for active. | To CN1 pin 31. |
| 22 | PB2 | I/O | Provides memory $\overline{\text{A}}$/B in. Low for selecting "A". | To CN1 pin 30. |
| 23 | PB1 | I/O | Provides BLK EN in/out. Stays low during BLK balance. | To CN1 pin 32. |
| 24 | PB0 | I/O | Provides WHT EN in/out. Stays low during WHT balance. | To CN1 pin 34. |
| 25 | TX OUT (PC7) | I/O | Control signal to select multiplexer IC6. | To pin 9 of IC6. |
| 26 | RX IN (PC6) | I/O | Control signal to select multiplexer IC6. | To pin 10 of IC6. |
| 27 | SCK I/O (PC5) | I/O | Control signal to select multiplexer IC6. | To pin 11 of IC6. |

| Pin No. | NAME | I/O | FUNCTION | CONNECTION |
|---|---|---|---|---|
| 28 | PC4 | I/O | Enables IC3 (window gen) ON/OFF. | To pin 11 of IC3. |
| 29 | PC3 | I/O | Provides BLK tracking command line. High sets BLK tracking mode. | To pin 14 of IC2. |
| 30 | PC2 | I/O | Provides G/BLKG switchover command. High sets green mode. | To pin 5 of IC2. |
| 31 | PC1 | I/O | Provides R/B switcher command. | To pin 7 of IC2. |
| 32 | PC0 | I/O | Provides G/ (R/B) switcher command. | To pin 6 of IC2. |
| 33 | $V_{DD}$ | I | +4.6V power supply. From +4.6V line. | From +4.6V line. |
| 34 | PD1 | I | Sample (DLY 0H) in. | From CN1 pin 19. |
| 35 | PD2 | I | Provides self-diagnosis mode ON/OFF control. | From switch S1 (check). |
| 36 | PD3 | I | Provides busy in from EE PROM IC17. | From pin 7 of IC17. |
| 37 | PD4 | I | Provides DATA in. | To pin 4 of IC17. |
| 38 | PD5 | I | Provides S2 (memory reset) in. | From switch S2. |
| 39 | $\overline{\text{INT}}$ 2 (PD6) | I | Provides audio CH2 IND ON/OFF signal in. | From pin 10 of IC4. |
| 40 | PD7 | I | COMP out input. | From pin 7 of IC7. |
| 41 | PE0 | O | Auto IND output. High enables IND. Not used. | N.C. |
| 42 | PE1 | O | Provides camera ready out. Low for active. | To CN1 pin 6. |
| 43 | PE2 | O | $\overline{\text{LENS}}$ close output. | To CN1 pin 18. |
| 44 | PE3 | O | Provides memory R/W status out. | To pin 3 of IC10. |
| 45 | PE4 | O | Provides CE (chip enable) out. | To pin 1 of IC17. |
| 46 | PE5 | O | Provides SCK (sync clock) out. | To pin 2 of IC17. |
| 47 | PE6 | O | Provides DATA out. | To pin 3 of IC17. |
| 48 | PE7 | O | SD output. | To Q3 base. |
| 49 | PF0 | O | Selects "A" of IC12 (multiplexer). | To pin 15 of IC12. |
| 50 | PF1 | O | Selects "B" of IC12 (multiplexer). | To pin 14 of IC12. |
| 51 | PF2 | O | Selects "C" of IC12 (multiplexer). | To pin 13 of IC12. |
| 52 | PF3 | O | Selects "$\overline{\text{EN}}$" of IC12 (multiplexer). | To pin 9 of IC12. |
| 53 | PF4 | O | IRIS REM output. | To Q1 base. |
| 54 | PF5 | O | Provides IRIS REM/$\overline{\text{LOCAL}}$ out. | To CN1 pin 38. |
| 55 | PF6 | O | Selects "STROBE" of IC11 (CHR GEN). | To pin 9 of IC11. |
| 56 | PF7 | O | Provides $\overline{\text{CHU}}$/CCU signal out. | To CN1 pin 44. |
| 57 | PG7 | I/O | CORR SIG output. | To pin 2 of IC9. |
| 58 | PG6 | I/O | | To pin 4 of IC9. |
| 59 | PG5 | I/O | | To pin 6 of IC9. |
| 60 | PG4 | I/O | | To pin 8 of IC9. |
| 61 | PG3 | I/O | | To pin 17 of IC9. |
| 62 | PG2 | I/O | | To pin 15 of IC9. |
| 63 | PG1 | I/O | | To pin 13 of IC9. |
| 64 | PG0 | I/O | | To pin 11 of IC9. |

**Table 8-1. Pin Allocation and Function**

The auto white balance data for each filter position are stored in the two (total eight) EEPROMs (IC17 : CXK1011P) which are connected to microprocessor IC14. The black tracking and auto black balance data are also stored in the EEPROM. EEPROM IC17 is an erasable/writable MNOS non-volatile memory with 64 words × 8 bit structure. It has the following features :

- +5V single power supply
- Full decode, 64 words × 8 bit structure
- Serial data transfer
- Rewrite by word or total chip rewrite
- Memory retention is more than 10 years
- TTL ICs can be directly driven
- Low power consumption (25 mW standard)

| PIN No. | TYPE | NAME | PIN DESCRIPTION |
|---|---|---|---|
| 1 | IN | $\overline{CE}$ | Chip enable input |
| 2 | IN | $\overline{SCK}$ | Synchronous clock input |
| 3 | IN | DI | Data input |
| 4 | OUT | DO | Data output |
| 5 | POWER | GND | Power (0V) |
| 6 | IN | $\overline{OSC}$ | Oscillator input |
| 7 | OUT | $\overline{BUSY}$ | Busy output |
| 8 | POWER | Vcc | Power (+5V) |

**Table. 8-2. Pin Assignment and Function**

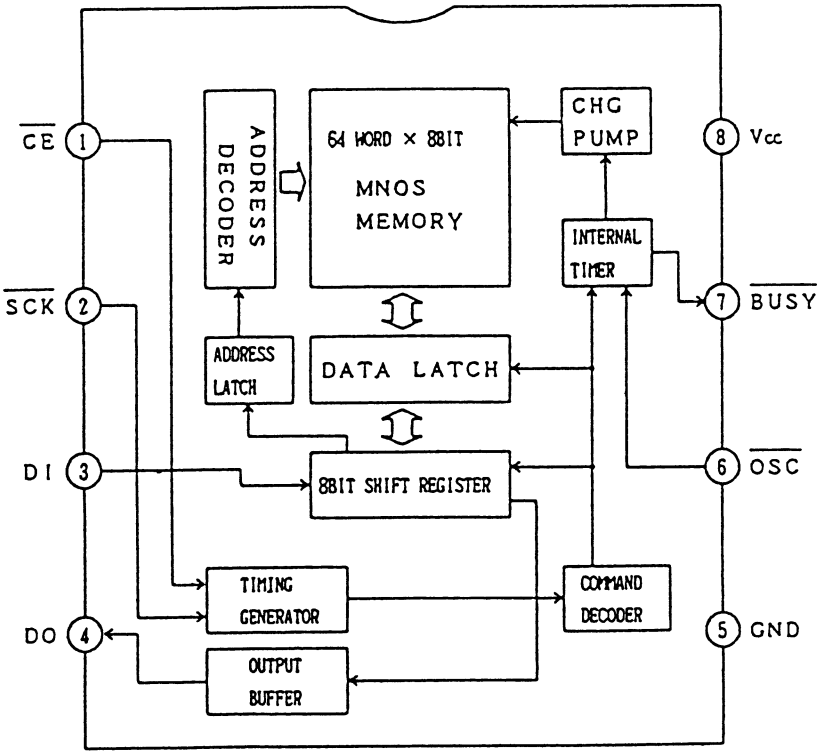



**Fig. 8-2. IC17 Block Diagram**

## 8-2. AUTO WHITE BALANCE CIRCUIT

Auto white balance is accomplished by the red and blue signal levels with the green signal until all three signals have the same amplitude when the camera shoots a solid white object.

The red, green and blue signals are supplied from the EN-79 board to the AT-49A board. The R−G and B−G signals are generated from three primary signal inputs. At the same time the red, green and blue signals are mixed to generate the Y signal. The R−G signal and the B−G signal are sampled during the peak value (white level) of the Y signal to generate error difference signals. The R−G and B−G error signals are A/D converted and sent to the microprocessor in the form of 8-bit digital data. The error signals are digitally calculated in the CPU to generate the error output GAIN CONTROL signals. The GAIN CONTROL signals are D/A converted and sent to the gain control circuit of processing amplifiers on the VA-83 board. The red and blue signal amplitudes are controlled until the "R:G" and "B:G" white levels are equal.

IC2 generates the G−G, R−G, B−G and G−BLKG signals required for auto black balance. The three primaries (red, blue and green signals) are input to pins 1, 2 and 3 of IC2 respectively. The color difference signals are generated inside IC2 and are fed at pin 19 of IC2 in accordance with each operating modes. The CTL signals output from pins 29, 30 and 31 of CPU IC14 are sent to pins 14, 5, 7 and 6 of IC2 to select the proper error difference signal.

When the WHITE BAL switch is set to ON, the CTL signal at pin 6 of IC2 input goes to a "Low" level and the CTL signal at pin 5 of IC2 goes "High". Then the G−G signal is generated inside IC2 and is output from pin 19 via differential amplifier (inside IC2). This G−G signal is sent to the sample-and-hold circuit via pin 4 of IC1 to sample the G−G signal by the Y peak signal.

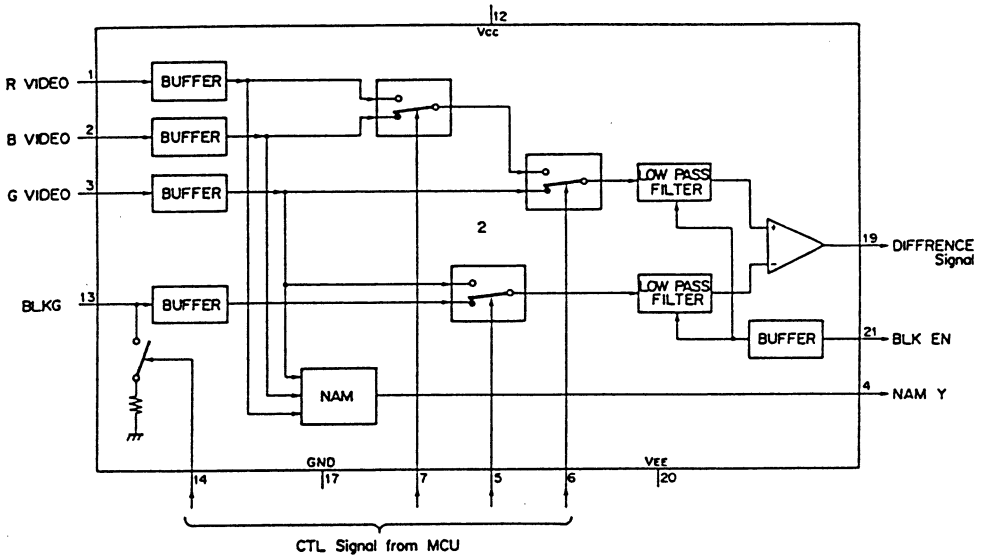



Fig. 8-3. IC2 Block Diagram

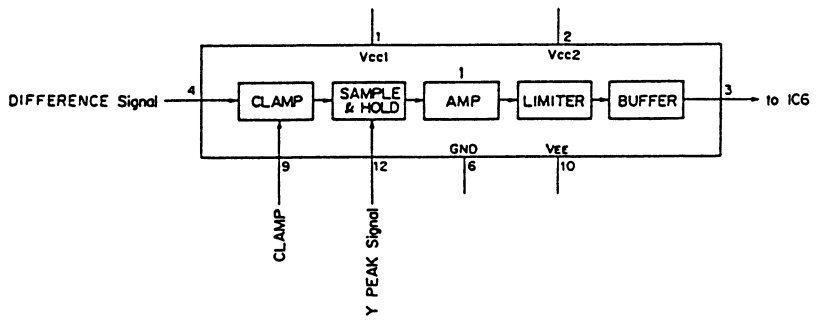



Fig. 8-4. IC1 Block Diagram

The horizontal and vertical parabola signals are supplied from the VA-83 board to pin 14 of IC3 to generate a window pulse with elliptical shape in the center scanning area occupying 70% of effective screen size. This window pulse is sent to the signal peak detector in IC3 so the peak value of the NAM Y signal is detected. The NAM Y signal is generated by IC21 and sent to pin 3 of IC3. The Y PEAK signal feeds to pin 10 of IC3.

The G−G signal output that is sampled-and-held by the Y peak signal is amplified and sent from pin 3 of IC1 to pins 6 and 13 of IC6. IC6 is the input signal selector for microprocessor IC14 which functions as a sequential A/D converter.

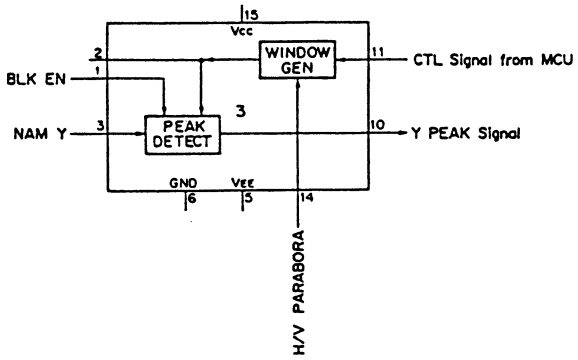



Fig. 8-5. IC3 Block Diagram

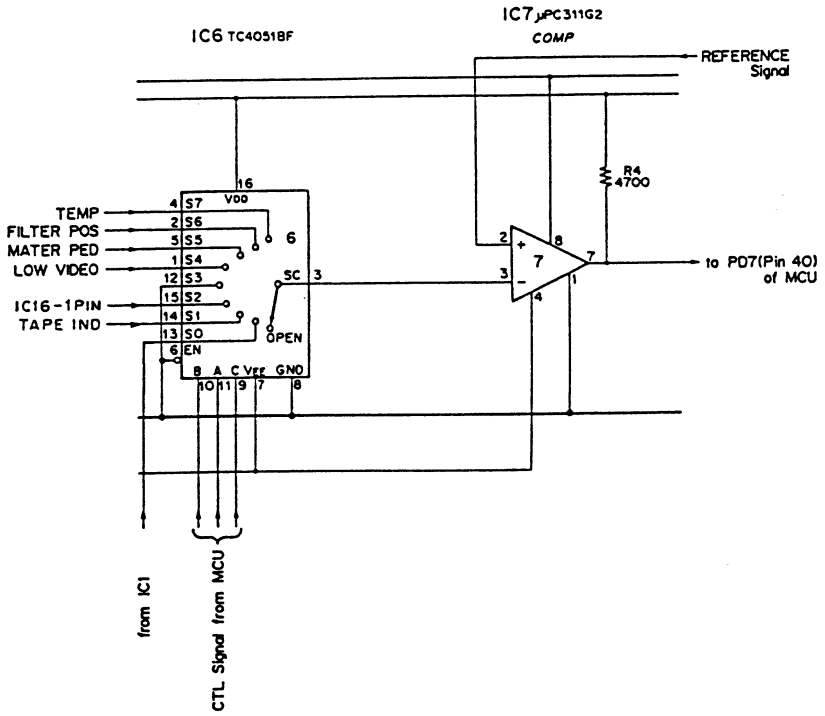



Fig. 8-6. Input Selector

Input signal selector IC6 receives not only the color difference signals, but also the filter position, master pedestal, LOW VIDEO, audio level and residual tape signals. The dc signal selected by IC6 is sent to pin 3 (inverting input) of IC7 from pin 3 of IC6. The pin 2 (non-inverting input) of IC7 receives the analog signal produced by converting the CPU digital output with D/A converter RB3. Comparator IC7 compares pin 2 input voltage with the CPU output reference voltage, and generates either an "H" or "L" level from pin 7 of IC7 to pin 40 of CPU IC14 (PD7). In the sequential A/D converter, the first comparison process determines the value of the MSB. The second comparison determines the 2nd MSB value. This comparison process is repeated eight times so the dc voltage input at pin 3 of IC7 is A/D converted to 8-bit digital data.

The G−G signal which has been converted to 8-bit digital data is stored in CPU IC14 as a reference signal. The G−G signal is used as a reference signal to minimize temperature elapsed time effects when B−G and R−G signals are generated. AFter the G−G voltage value is stored in the CPU, level "H" is supplied from pins 30, 31 and 32 of IC14 to generate the R−G signal. The R−G color difference signal is supplied from pin 19 of IC2. This signal is converted to an 8-bit digital signal and stored in the CPU like the G−G signal. The G−G and R−G signal amplitudes are compared in the CPU. If the error data between these two signals is less than one bit (LSB one bit of the 8 bit data), it is assumed that good white balance is maintained.

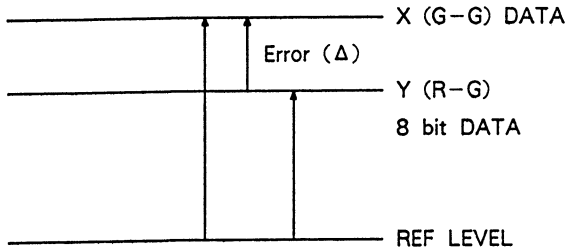



**Fig. 8-7. Comparison Voltage**

While good white balance is maintained, the CPU does no correction and proceeds to the next step. When correct white balance is not attained, the CPU generates a correction signal R GAIN CONT (8-bit digital data) which varies red signal amplitude until correct white balance is attained. RB3 is the D/A converter ladder resistor block. The D/A converted output analog voltage is sent to the primary signal gain control circuit in the VA-83 board.

As described above, the CPU generates an 8-bit digital data signal which changes its output data (00H to FFH) in accordance with the white balance error value. If the error between the R−G and G−G signals is too large so even 00H through FFH cannot produce the correct white balancing, NG is displayed in the viewfinder.

The D/A converted R GAIN CONT signal is buffered by IC9 and sent to pin 8 of analog switcher IC12. IC12 selects the proper data to be stored in the CPU as selected by the control signal from pins 49 through 52 of CPU IC14.

| IC12 PIN No. | OUTPUT |
|---|---|
| 19 | R GAIN CONT |
| 17 | B GAIN CONT |
| 18 | R BLK CONT |
| 20 | B BLK CONT |
| 5 | R PED CONT |
| 6 | MASTER PED CONT |
| 2 | G BLK CONT |
| 7 | B PED CONT |

**Table 8-3. IC12 Output Signals**

The various analog correction signals are supplied from analog switcher IC12. The R GAIN CONT signal (+2.3±2.3 Vdc) is supplied from pin 19 of IC12 to the VA-83 board. The red signal amplitude is repeatedly corrected until the signal difference between the red and green signal becomes less than one bit. After correct white balance of the red signal is attained, the CPU advances to the blue signal white balancing operation. When the blue signal attains the same amplitude as that of green signal, the correction data is stored in the IC17 (EEPROM) and the white balance operations are complete.

## 8-3. AUTO BLACK BALANCE CIRCUIT

The auto black balance operations are carried out in the sequence of section 8-3-1, 8-3-2 and 8-3-3.

### 8-3-1. Lens Iris Closing Operation

When the BLACK BAL switch is ON, pin 23 of CPU IC14 goes to a "Low" level and pin 43 of IC14 supplies "High" to the auto iris control circuit (located on the SG-152 board to close the lens iris). Incident light is blocked and the auto black balance operation can be started.
G−BLKG signal detection indicates whether the lens iris is completely closed or not. When the BLACK BAL switch is ON, the CPU generates a "Low" level from pins 30 and 32 of IC14 to produce the G−BLKG signal from pin 19 of IC2 (used for iris close determination).
Also, if the green signal pedestal level is set too low, the green signal will be incorrect for detection of iris closure. In order to prevent this, the BLKG signal level is reduced when the AUTO BLACK BAL switch is set ON by supplying the "Low" level from pin 29 of CPU IC14 to pin 14 of IC2. At the same time, the green signal pedestal level is raised automatically by shifting the master pedestal control signal.

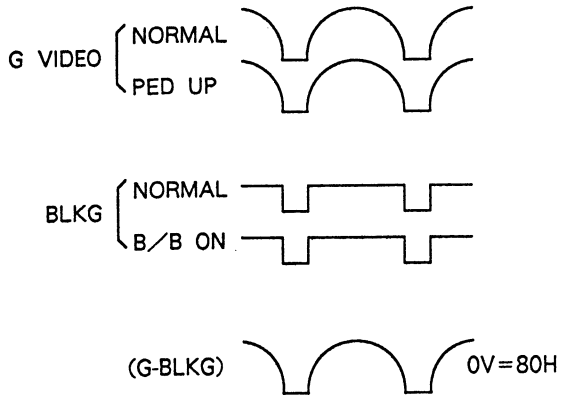



Fig. 8-8. Auto Black Balance Waveform

The G−BLKG signal of the differential amplifier output is A/D converted and stored in the CPU. When this G−BLKG signal becomes 0V (80H), the lens is detected as closed. The differential amplifier output is then A/D converted twice successively. If the level difference during these operations is within ±1 bit digitally, the lens is completely closed.

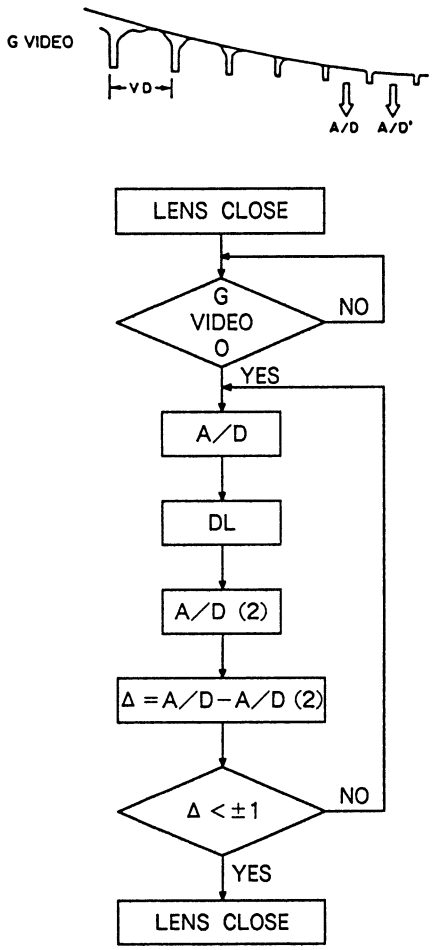



Fig. 8-9. Lens Iris Closing Operation Flowchart

### 8-3-2. Black Tracking Operation

Even though the lens iris is closed, the pre-amplifier output signal includes the CCD dark current component.
For example, when the GAIN UP switch is operated from 0 dB to +9 dB, the dark current component is also amplified by the gain amplifier on the VA-83 board to produce an error in the black level tracking. In order to prevent the black tracking error, auto black tracking operation is executed first on the green signal when the GAIN select switch is used while the iris is closed. Auto black track is then executed on the red signal and the blue signal to stabilize the black (pedestal) level of the camera output signal. When the lens iris is completely closed, pin 29 of CPU IC14 returns to "High" so the BLKG signal passing through IC2 returns to normal level and the G-BLKG signal is fed to pin 19 of IC2.
When the GAIN-UP switch is set to the 0 dB position, the A/D converted data representing the 0 dB G-BLKG signal level is stored in the CPU. Then, when the GAIN-UP switch is set to the +9 dB position, the +9 dB gain-up control signal is supplied from pin 15 of CPU IC14 and the primary signals' gain in increased by +9 dB in the amplifiers on the VA-83 board. Then the digital data representing the +9 dB G-BLKG signal level, is stored in the CPU, and compared with that of 0 dB mode. If the G-BLKG signal level difference ($\Delta$) between 0 dB mode and +9 dB mode, is supplied as is, the pedestal level after correction will be fixed to the data of +9 dB mode. 1/2 ($\Delta/2$) of the level difference is sent to the VA-62 board as a correction signal. The G-BLKG signal level difference between 0 dB mode and +9 dB mode is again compared, and the correction signal of $\Delta/2$ is output. By repeating this operation several times, the pedestal level in the 0 dB mode and +9 dB mode are made the same. After the level difference $\Delta$ becomes less than $\pm 1$ bit, the CPU judges that the green signal black track is correct. The CPU advances to red signal black tracking then finally to blue signal tracking. In this way, all black tracking is completed.

### 8-3-3. Auto Black Balance Operation

After the lens is closed, the signal level difference between the green channel black signal and the red channel black level is detected. Then the black level difference between the green and blue channels is detected. At the same time, pedestal control signals (R PED CONT and B PED CONT signals) are sent to the VA-83 board where the pedestal levels of red, blue and green signals are made equal.

## 8-4. FILTER POSITION DETECTOR

The white balance data for filter positions No.1, No.2, No.3 and No.4 (8 different types of data), are stored in the EEPROM. Position signals for the four filters are supplied from pin 14 of CN1 on the AT-49A board in the following voltages :

- Filter-1 : $0 \pm 0.5$V
- Filter-2 : $1 \pm 0.5$V
- Filter-3 : $2 \pm 0.5$V
- Filter-4 : $3 \pm 0.5$V

Filter positions are detected by A/D converting these input voltages.

The gain control signal of the red and blue channel signals stored in the EEPROM (and used for white balance operation), are selected by the filter position signal. The MEMORY A/B are fed to pin 22 of IC14.

## 8-5. RESIDUAL TAPE INDICATOR CIRCUIT

This equipment has a function to indicate remaining amount of tape in the viewfinder. The residual tape (TAPE IND) signal is supplied from the SY-117A board to pin 7 of CN1 on the AT-49A board where it is A/D converted to display remaining tape on the viewfinder. Display results corresponding to the TAPE IND signals are as follows :

- 0V : no display
- 1.2V : "5-0"
- 2.4V : "10-5"
- 3.6V : "15-10"
- 4.8V : "FU-15"

## 8-6. AUDIO LEVEL INDICATOR

This equipment has a function to display the audio channel-1 recording level on the viewfinder with characters. The display of audio channel-1 recording level can be switched ON/OFF by the AUDIO IND ON/OFF switch.

DC voltage of the audio channel-1 signal supplied from the AU-97 board is filtered by C7 and C6 on the MB-173A board and sent to pin 13 of CN1 on the AT-49A board. The AUDIO IND ON/OFF switch on the viewfinder is connected to pin 13 of CN1. If the AUDIO IND switch is set ON, a dc voltage is added to the audio channel-1 signal input to pin 13 of CN1 via R120 on the AT-49A board. When the AUDIO IND switch is set OFF, the audio channel-1 signal at pin 13 of CN1 becomes an ac signal only. The dc voltage is detected in this circuit and used as the ON/OFF control signal for the level indication. The AUDIO IND ON/OFF signal with its ac signal filtered by R21 and C29, is inverted by IC4 and sent to pin 39 of CPU IC14.

The audio channel-1 signal is full-wave rectified by IC16. The rectified voltage is sent to multiplexer IC6 where it is A/D converted and sent to the CPU. Thus the audio level indication in the viewfinder is changed in accordance with the rectified signal data input to the CPU. The display level can be adjusted by RV4. A " : " mark is indicated on viewfinder when a 0.7 Vp-p signal is input.

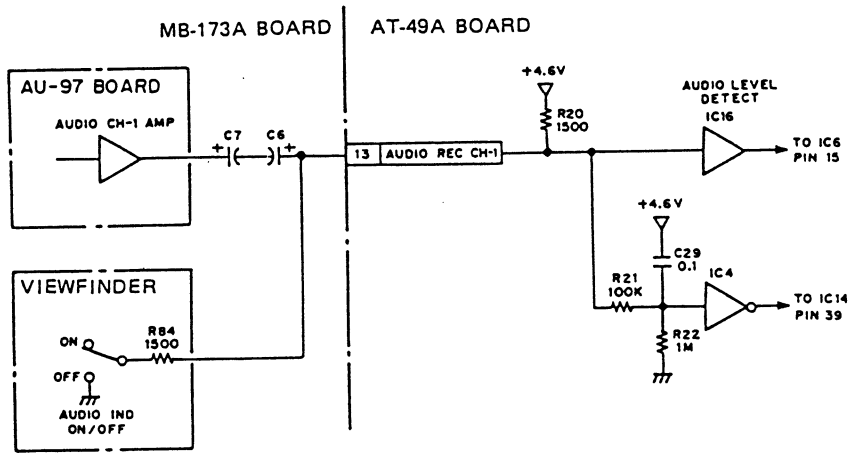
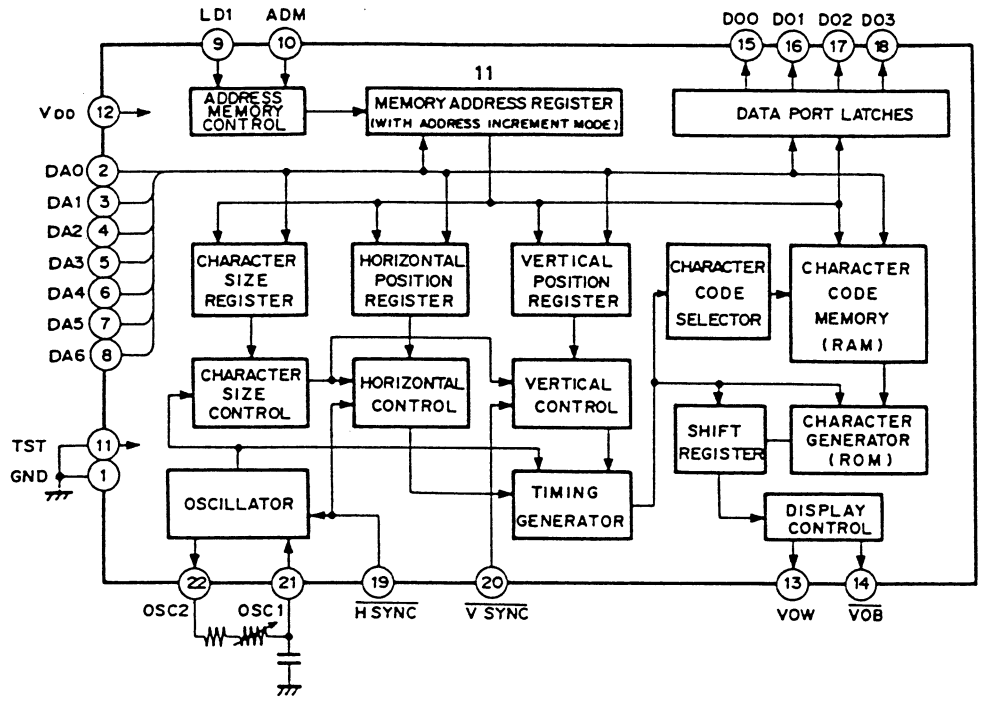



**Fig. 8-10. Audio Level Indicator**

## 8-7. CHARACTER GENERATOR

IC11 (MN1237AD with built-in ROM) generates characters to be displayed in the viewfinder. Various display data such during white balance mode (WHT : OP), black balance mode (BLK : OP) and operation result (WHT : OK, WHT : NG), are supplied from the CPU to IC11 terminals DA6 through DA0. The horizontal display position of the viewfinder can be adjusted by RV1.



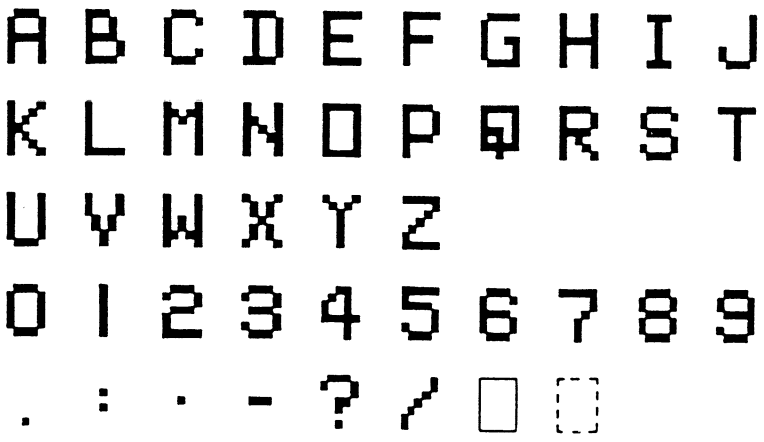




Fig. 8-11. IC11 Block Diagram and Display Characters

## 8-8. SELF-DIAGNOSTIC FUNCTION

### 8-8-1. Self-diagnostics in the Camera Block

When switch S1 (CHECK) on the AT-49A board is set to the ON position, the camera block goes into the self-diagnostic mode. When the AUTO WHT/BLK switch is set to the WHT position, step 1 is initiated. Thereafter all steps to 5 are automatically executed. When the DIAGNOSTIC switch is pressed, the results of the camera self-diagnostic can be seen in MODE 4.

OPENING MESSAGE

```
-SELF DIAG.-
PUSH AWB. SW.
PROCEED TO
NEXT STEP
```

If AUTO WHITE switch is pressed set to ON position, checks are started automatically in the following sequence :

STEP 1

R/G-CH GAIN CHECK

```
-SELF DIAG.-
STEP 1
R.GAIN : OK
PUSH AWB. SW.
```

- Use the TEST SAW signal or view a proper object.
- The display changes from R GAIN to B GAIN.
- OK or NG is displayed.

STEP 2

R/G/B-CH BLACK SET CHECK

```
-SELF DIAG.-
STEP 2
R.BLK. : OK
PUSH AWB. SW.
```

- Lens is closed.
- The display changes from R BLACK to B BLACK to G BLACK.
- OK or NG is displayed.

STEP 3

R/B-CH PEDESTAL CHECK

```
-SELF DIAG.-
STEP 3
R.PED. : OK
PUSH AWB. SW.
```

- Lens is closed.
- The display changes from R PED to B PED.
- OK or NG is displayed.

STEP 4

OK INDICATOR CHECK

```
-SELF DIAG.-
STEP 4
AUTO IND OK?
PUSH AWB. SW.
```

- Indicator in VF is remains lit about 5 seconds.
- If indicator does not light, it is judged to be burned-out.

STEP 5

FUNCTION SWITCH CHECK

```
-SELF DIAG.-
STEP 5
SET 18 dB : OK
PUSH AWB. SW.
```

- The function switch operations are displayed in the following sequence. Use the appropriate switch setting. 18 dB → 9 dB → BARS → TEST → DCC → FP.INH → WHT A/B → WHT PRST.
- OK or NG is displayed.

**Note** : Warning display in step 2 and step 3.

```
STEP 3
LENS :
   NOT CLOSED
```

- This indicates that the lens is not closed.
- The warning remains until the lens is closed.

**Fig. 8-12. Self-Diagnostic**

### 8-8-2. VTR Self-diagnostic by the Display in Viewfinder

When the DIAGNOSTIC switch on the left side of the equipment is pressed, the VTR goes into self-diagnostic mode. The results of VTR and the camera self-diagnostic are displayed by letters shown in the viewfinder or by indicators.
The character commands for VTR self-diagnostics to be displayed in the viewfinder are supplied in serial data format from the CPU on the SY-117A board to pin 3 of CPU IC14 on board AT-49A. When new data arrives, IC14 refreshes display data to be transferred to character generator IC11. Because the serial communication data line between the CPU on the SY-117A board and the CPU on the AT-49A board is also used with remote control unit RM-P3, priority is set as follows :

1. After an RM-P3 has been connected (even when subsequently disconnecting the RM-P3) the CAMERA READY signal at pin 4 of CPU IC14 on the AT-49A board remains at level "H" unless power is reset by an ON/OFF operation. Therefore, a BUSY status is sent to the CPU on the SY-117A board and the self-diagnostics mode cannot be received.

2. When an RM-P3 is connected during self-diagnostics, the equipment goes into remote control mode after self-diagnostics is completed. If the RM-P3 is manipulated during self-diagnostics, erroneous equipment operation may occur.

# SECTION 9
# SG-152 BOARD

## 9-1. OUTLINE

The SG-152 board consists of the following circuits :
- Sync signal generator
- SC phase adjustment circuit
- Gen lock circuit
- Sub regulator
- Auto iris circuit

## 9-2. TYPES OF SYNCHRONOUS MODES

(1) Internal synchronous mode
In the internal synchronous mode, when no GEN-LOCK signal is applied from an external source, the SG-152 board generates and outputs various sync signals such as SC, BF, CF, HD, VD and SYNC using the 17.7 MHz (4fsc) signal as the reference clock signal.
The VCO X1 oscillates the 17.7 MHz (4fsc) clock by applying a 2.5 Vdc. The 4fsc signal enters pin 10 of IC7. The IC7 generates the SC signal and an fH signal using the 4fsc signal as the reference.
The IC7 compares the phase of the sync HD signal generated by IC7 using the 14 MHz (908fH) signal as the reference with that of the fH signal referenced 4fsc.
The output signal of H phase comparator is applied to the VCO on the TG board inside the CCD block as the VCO CONT signal via buffer IC5 and limiter D1. The VCO generates the central oscillating frequency 29.5 MHz as the CCD drive clock. This clock signal is divided by two and input to SG-152 board.
IC21 converts the 14.75 MHz (1/2×29.5 MHz ; 944fH) into the 14.18 MHz (908fH), and H phase lock loop is formed to synchronize the timing generator for CCD with the sync generator.

(2) External synchronous mode
When a GEN-LOCK signal is input from an external source, the signal is input to pin 1 of sync separator IC1 and separated into the CHROMA signal and SYNC signal in IC1. The CHROMA signal is sent to pin 4 and the SYNC signal is sent to pin 17 of IC3. When IC3 detects the SYNC signal, the external synchronous mode is set and pin 11 goes high. The two switches of IC23 (1/3, 3/3) are set to the pin 13 and pin 3 positions.
The IC3 compares the phase of external SC with SC generated in IC7 using 4fsc signal as the reference. The result of comparison (SC COMP) output from pin 1 of IC3 is input to IC5 (3/4, 4/4), and passes through the low-pass filter, DC amplifier, and upper limiter in D3. It is then output from pin 14 of IC4 (2/2) as a VCO CONT signal and is applied to X1 (4fsc VCO). Its oscillation frequency is controlled so that it matches the SC phase of the GEN-LOCK signal.
The H phase comparator is also provided in the IC3, and it compares the phase of EXT SYNC signal with that of HD signal generated in IC7 using 908fH signal as the reference.
The comparison signal (H COMP) is output from pin 9, and applied to the 29.5 MHz VCO with same manner as the internal synchronous mode.

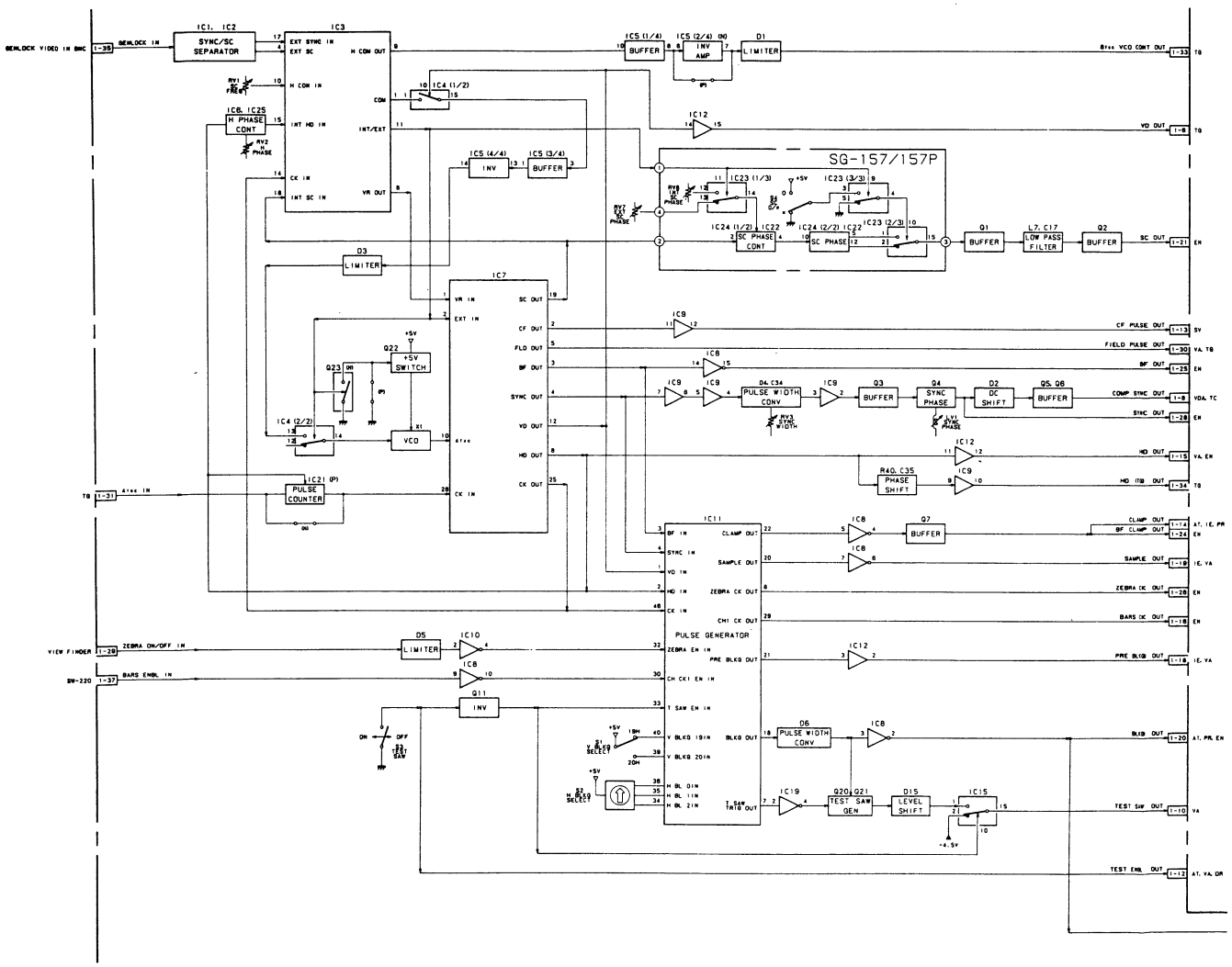



Fig. 9-1. Sync Generator

## 9-3. SC PHASE ADJUSTMENT CIRCUIT

This circuit has function to change the phase of output subcarrier signal from 0 degree through 180 degrees. Pulse width (phase) of subcarrier signal from pin 19 of IC7 is changed in IC24 in accordance with the input signal voltage level that is sent to pin 2 of IC24 through pin 2 of the SG-152 board. In internal sync lock mode, subcarrier pulse width (phase) is changed by the voltage determined by RV8 which is connected to pin 12 of IC23. In external sync mode, subcarrier pulse width (phase) is determined by the voltage set by RV7 which is connected to pin 13 of IC22.

The phase-adjusted subcarrier signal is inverted its phase and output from pins 5 and 12 of IC24 and sent to pins 1 and 2 of IC23. Either one of two signals is selected by the control signal input at pin 10 of IC23. In external sync lock mode, the control signal input at pin 10 of IC23 is selected by the switch S4 (0° /180° ) connected to pin 3 of IC23. Thus, by combined use of S4 switch where subcarrier phase can be 180 degree phase-inverted, and potentiometer RV7 that provides fine adjustment of subcarrier phase, the EXT SC phase can be adjusted from 0 degree through 180 degrees. Subcarrier signal after phase adjustment is output from pin 15 of IC23, buffered by Q1 and sent to low-pass filter (L7, C17). Harmonic component is removed by low-pass filter i.e., subcarrier signal is wave shaped into sinusoidal wave by this filtering. The output subcarrier is sent out via buffer Q2.

## 9-4. GEN-LOCK CIRCUIT

When inputting the VBS signal the GEN LOCK VIDEO IN connector, the signal is automatically synchronized to the VBS signal's sync and subcarrier phase and all output timing pulses are gen-locked (except sub-carrier).

The GEN-LOCK VIDEO signal sent to pin 35 of CN1, is sync-separated into the sync signal and the sub-carrier signal by IC1. The sync signal is sent to pin 17 of IC3. When IC3 receives the external sync input signal, external sync mode is automatically established. Then, the phase of the external sync input at pin 17 and the INT HD signal at pin 15 are phase-compared. The detected phase error voltage is generated and sent to the VCO on the TG-57 board from pin 9 as the H COMP OUT signal (29.5 MHz VCO CONT signal).

The vertical sync phase is synchronized by feeding the vertical reset pulse (obtained by detecting vertical blanking from external sync with IC3) to IC7. During gen-lock, subcarrier is generated from 4fsc output from the VCO and the EXT SC phase and INT SC phase are compared and synchronized in simillar to the sync signal.

IC11 is a pulse generator which generates pulses as shown in Fig. 9-3. When the 4fsc signal is supplied from the TG-57 board, the burst flag, sync, VD and HD signals are delivered from IC7. In addition, a sync pulse is sent from pin 4 of IC7 to the EN-79, VDA-11 and TC-48A boards. The width of this pulse is adjusted by D4, C34 and RV3. The rise and fall times are controlled by Q4 and LV1.

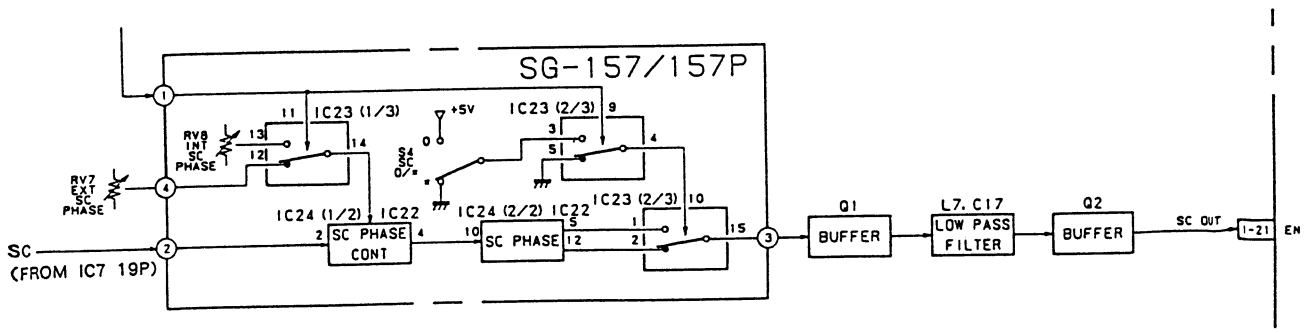



Fig. 9-2. SC Phase Adjustment

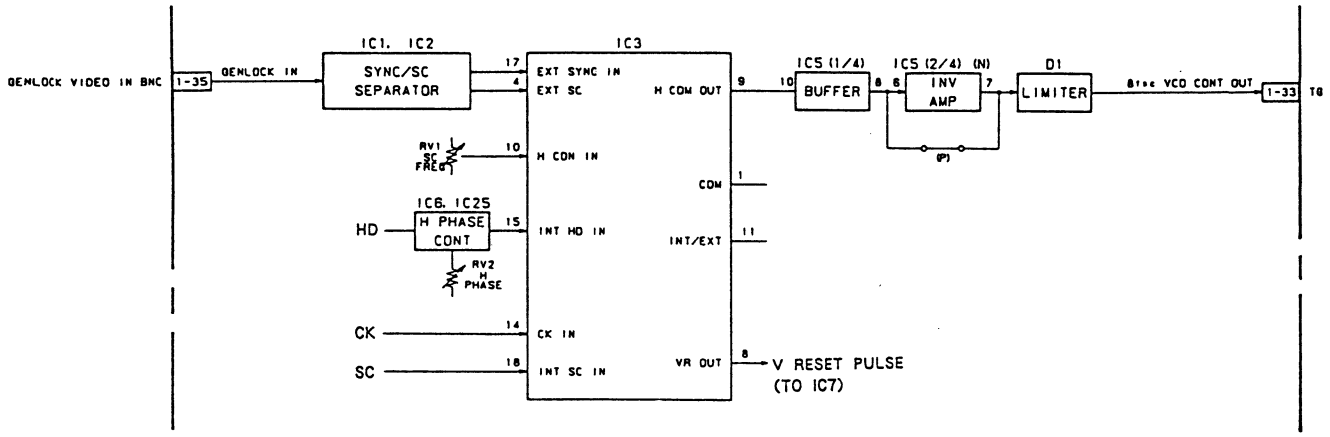



Fig. 9-3. Gen-Lock Circuit Block Diagram

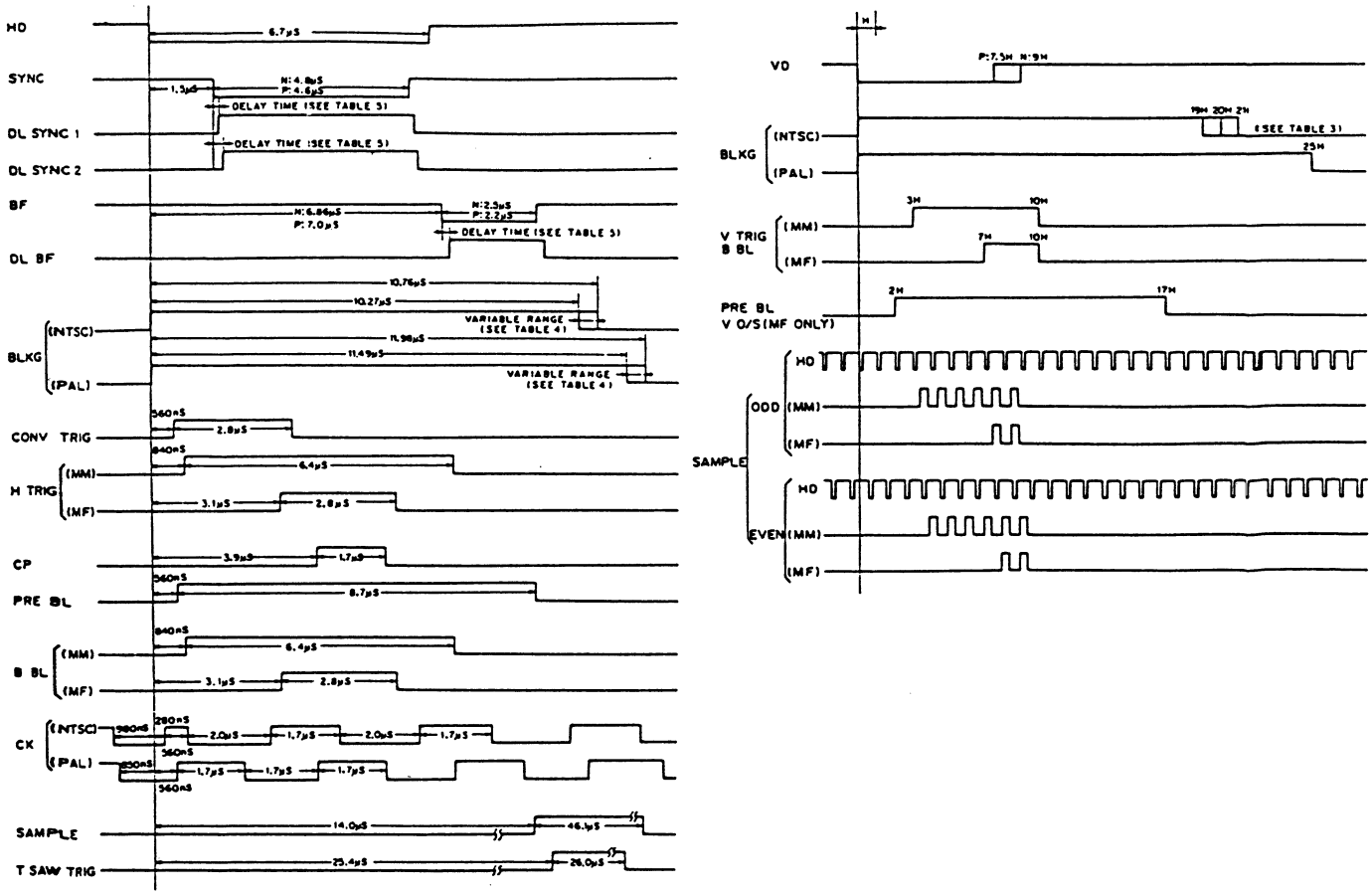



Fig. 9-4. Output Pulse Timing Chart

## 9-5. SUB-REGULATOR CIRCUIT

The SG-152 board has the following power regulator circuits :

- +8.5V
- +4.6V
- +4.7V
- −4.5V

The levels of +8.5V, +4.6V and −4.5V are used as the power supply voltages in each circuit board. The +4.7V power is used in the DR-84 board which contains the CCD imager block.

The sub-regulator circuit is equipped with a power save circuit which inhibits operation of the +8.5V/ +4.6V/−4.5V regulators when the VTR goes into the playback mode and the PB ON signal at pin 11 of CN1 goes "Low".

The +4.6V regulator consists of IC13 and Q10. The −4.5V regulator consists of IC13 and Q9. The reference voltage for the +4.6V regulator is generated from +8.5V. The reference voltage for the −4.5V regulator is generated from +4.6V. Therefore, when the PB ON signal goes "Low", the +8.5V, +4.6V and −4.5V regulators are all inhibited.

During the power save mode (while in VTR playback), the power supplies used in the camera are disabled. However a signal is required for the VTR, even during playback. So power is supplied to the sync signal generator on the SG-152 board, CCD block and the 29.5 MHz VCO on the TG-57 board during playback.

## 9-6. AUTO IRIS CIRCUIT

The NAM Y signal supplied from the PR-132 board, is input to pin 38 of CN1 on the SG-152 board, buffered by Q13 and then sent to pin 5 of IC17. When Q15 is switched by the V SAW signal, pin 5 of IC17 is grounded so high picture levels are prevented from triggering auto iris operation by the NAM Y signal. The NAM Y signal is passed through IC17's internal buffer, and is rectified by the peak value (D10 and C57) and the average value rectifiers (C56 and R83). The peak rectifier and average rectifier outputs are mixed. The mixing ratio is adjusted by RV6 (IRIS MODE). By controlling the mixing ratio with RV6, the iris control mode can be changed from peak value to average value mode. The iris control signal is amplified at pin 13 of IC17 and is again input to pin 3 of analog switcher IC15. The auto iris offset can be adjusted by RV5.

When remote control RM-P3 is used for iris control, the IRIS REM/LOCAL signal from the AT-49A board activates pin 5 of IC15 so the IRIS REMOTE signal from the AT-49A board is used as the iris control signal.

When a lens with 12-pin connector is used, the IRIS POSI signal (feed-back signal for iris control) from the lens output is fed-back to pin 13 of IC17 so iris response time is shortened and iris hunting is suppressed.

When a lens with 6-pin connector is used (this does not have an IRIS POSI signal), R96, R99 and C62 are added in parallel with the IC17 feed-back resistor (by IC15) to reduce gain.

When the LENS CLOSE IN signal from the AT-49A board goes "Low", +5V is supplied from pin 4 of IC18. Q16 is turned ON by this signal so the IRIS CONT signal is grounded, the AUTO +5V becomes +5V and the lens is closed.

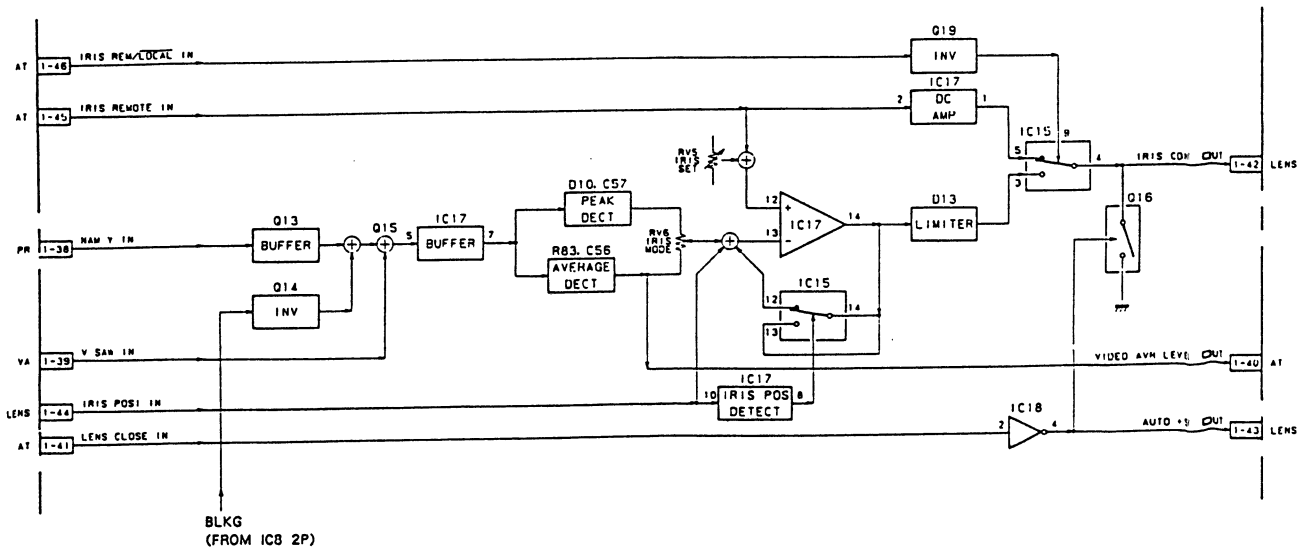



Fig. 9-5. Auto Iris Circuit Block Diagram

# SECTION 10
# VIEWFINDER

## 10-1. OUTLINE

The viewfinder consists the CRT and the following circuit boards :

- VF-32
- LP-40
- LP-42
- SW-260
- VR-67

## 10-2. BATTERY ALARM LED DISPLAY

When the battery output voltage drops below 11.3 Vdc, the battery alarm LED blinks. When voltage drops below 11.0 Vdc, the LED stays on. The blink/steady voltage is controlled by the BATT IND signal supplied from the SY-117A board.

## 10-3. REC/TALLY LED DISPLAY

The REC/TALLY LED lights during recording and blinks when remaining tape is less than 2 minutes. The steady/blink voltage is controlled by the CTL REC signal.
The REC/TALLY LEDs are installed in the front interior of the viewfinder and also in the rear of handle. Brightness of the tally LED in the front of viewfinder can be switched to "H/L/OFF" by switch S1 on the SW-260 board.

## 10-4. CRT CONTROL CIRCUIT

The video signal to be displayed in the viewfinder is supplied to pin A5 of CN1 on the VF-32 board from the MB-173A board. The video signal is separated to the video signal output and signal output for synchronization. The video signal is sent to the VR-67 board where its contrast level is adjusted by RV1. The signal is again returned to the VF-32 board. Then the video signal is buffered by Q1 and takes two output paths.
One video output is delayed by DL1 for 120 nsec, amplified by Q2 and sent to Q3.
The other video output signal is passed through low-pass filter CV1 and L3 and sent to Q4. The differential amplifier consists of Q3 and Q4. This amplifier obtains the difference between the delayed signal and the signal whose frequency response is decreased by the filter. This output from Q5 as the peaking signal, dc components of this signal are cancelled by RV8. The PEAKING signal is sent to the VR-67 board where level is adjusted and the signal is mixed with the Q3 buffer output video signal to emphasize high frequency components. The emphasized video signal is amplified by Q6, buffered by Q10, clamped by Q7 and sent to G1 on the CRT.
Meanwhile, the video signal for synchronization is clamped by C26 and D8 and sent to pin 11 of IC1. The input signal is sliced at dc level at input pin 10. Thus the sync signal is separated. Separated sync is sent to the phase detection circuit (horizontal AFC circuit) in the IC, so a positive polarity sync pulse is output from pin 8 of IC1. The positive polarity signal pulse from pin 8 of IC1 is integrated by R49 and C37 to produce the vertical trigger pulse which is sent back to pin 7 of IC1. R55, R56, RV5 and C40 are the time constant circuit to determine the width of the vertical trigger pulse. The vertical hold frequency can be changed by RV5.
A sample of vertical deflection coil current is fed back to pin 4 of IC1 as voltage where the correction vertical linearity is adjusted by RV7. Vertical deflection size is adjusted by RV4 and RV6.
The vertical oscillation signal, after lineality correction, is balanced by the dc/ac amplitude signal from pin 2 of IC1. This takes two output paths. One output is sent to IC4 from pin 18, gated by a NOR-gate with the horizontal deflection pulse, and is added to the main video signal as the vertical blanking signal. The other output is sent from pin 1 to the vertical drive circuit of Q13 through Q15, to generate a sawtooth wave to provide drive current through the vertical deflection coil.

The AFC GATE circuit inside IC1 is a differential amplifier phase detector to compare the separated sync pulse with the flyback pulse from pin 12. Error voltage output from phase comparison is supplied from pin 13 to pin 14 of IC1 through low-pass filter C31, C32, R43 and R45.
Since the "H" level of CCIR/EIA detection signal is fed to pin B5 of CN1 in the PAL system, Q12 is turned OFF so R46 is disconnected. So, a rectangular pulse is generated from the error voltage of the horizontal oscillation pulse The time constant is determined by R48, RV3 and C35. The signal is output as the horizontal drive pulse from pin 16.
To prevent X-ray radiation, the horizontal drive pulse output is inhibited when the power supply voltage to the flyback transformer becomes more than 13V (normally 9V).
The horizontal drive pulse output from pin 16 of IC1 is sent to the horizontal drive circuit of IC3 and Q8. Then, the flyback pulse is generated by switching Q8. Linearity of horizontal deflection coil is adjusted by R69 and L2. Q16 and IC2 are the horizontal size circuit where the horizontal size is adjusted by RV1. RV1 varies the voltage at pin 2 of IC2 which changes the power supply voltage of flyback transformer T1. Q9 and IC2 is the high tension stabilizer. The dc voltage is determined by RV2 is sent to pin 6 of IC2 while pin 5 of IC2 receives the rectified and tension separated output voltage from pin 6 of T1 (flyback transformer). These two voltage
levels are compared so an error voltage is output from pin 7. The error voltage is sent to the gate of Q9. The reactance including C16 is changed so the levels of the drive pulse and the flyback pulse (T1 output) are changed, therefore high tension is stablized. T1 includes the multiplier circuit and 6 kV dc is output directly to the anode of the CRT from T1. The output at pin 6 of T1 is rectified by D5 and C21 and is sent to the CRT as G2 voltage. H1 and H2 voltage are supplied from pin 1 of T1 and pin 5 of T1.

# VTR BLOCK

# SECTION 1
# MECHANISM BLOCK

## 1-1. OUTLINE OF MECHANISM

Mechanism of this equipment is designed aiming at the small size, light weight and good serviceability. Main features of this mechanism are listed as follows.

**[Small Size and Light Weight]**
- Slide-type movable reel table
- Small diameter head drum
- Magnesium die-cast chassis
- Good weight-balanced mechanism
- LCD audio level indicator
- Weight 6.9 kg (with BCT-20, NP-1, viewfinder, ×13 standard lens)

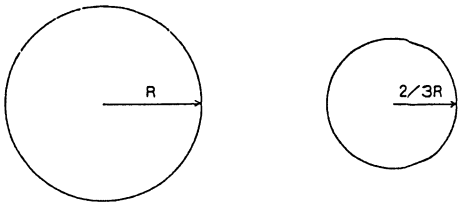
**[Reliability]**
- Solenoid-less mechanism
- Micro-switch-less mechanism
- Toothed timing belt
- No harness (Mother board and card boards are connected with 50P connector, and all printed circuit boards are plug-in type.)
- Plug-in type head drum assembly

**[Serviceability]**
- Skeleton-structured frame (it can be disassembled-assembled to six directions.)
- Disassembled-assemble type mechanism
- Manual eject system
- Mechanism can be removed by four fixing screws.
- All printed circuit boards are card board type.

## 1-2. HEAD DRUM

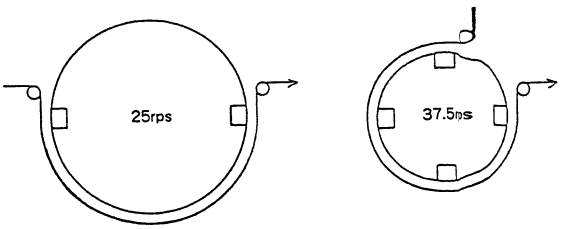
### 1-2-1. Outline of Head Drum

Head drum has the following specifications.
- Diameter : 2/3 of conventional equipment (see Fig. 1-1.)
- Rotating speed : 37.5rps (see Fig. 1-2.)
- Wrap angle : 270° (see Fig. 1-2.)




Conventional equipment BVW-300P

**Fig. 1-1. Comparison with Conventional Equipment (Diameter)**




Conventional equipment BVW-300P

**Fig. 1-2. Comparison with Conventional Equipment (Wrap angle, Rotating speed)**

### 1-2-2. Recording System

The head drum assembly consists of an upper drum and a lower drum containing rotor, coil inside. Rotary transformers are built-in at the center of head drum assembly. The PG coil is installed outside the drum assembly. The upper head assembly contains four Y (luminance) signal video heads of CH-1 through CH-4 and four chroma signal video heads of CH-1 through CH-4, totaling eight video heads.

Conventional VTR has the two video heads fundamentally that are located 180° apart each other. Each conventional head picks up the playback signal that are switched alternately to have continuity of channel-A output and channel-B output. In this equipment, the track-A is recorded by separate two video heads alternately and also the track-B is recorded by other two video heads alternately so as to maintain signal continuity on the recorded tracks. Since, the angle of "tape wrap around the drum" is 270° , when the CH-1 head (the first head) has completed to write down signal, the CH-2 head that is positioned 90° phase-advanced (i.e., 270° phase delayed position) starts to write signal. And then, when CH-2 head has completed to write down signal, the CH-3 head starts to write down signal. These four video heads are controlled in such a manner. The track-A is recorded by CH-1 and CH-3 video heads while the track-B is recorded by CH-2 and CH-4, alternately.

The RF alarm signal detection is carried out by using the video head that is opposite to the recording video head that has the least RF interference from the recording video head. The record/playback head amplifier use the highly integrated ICs that are located inside head drum. The special video head equipped with center tap is used in this equipment to have higher gain and high S/N ratio.

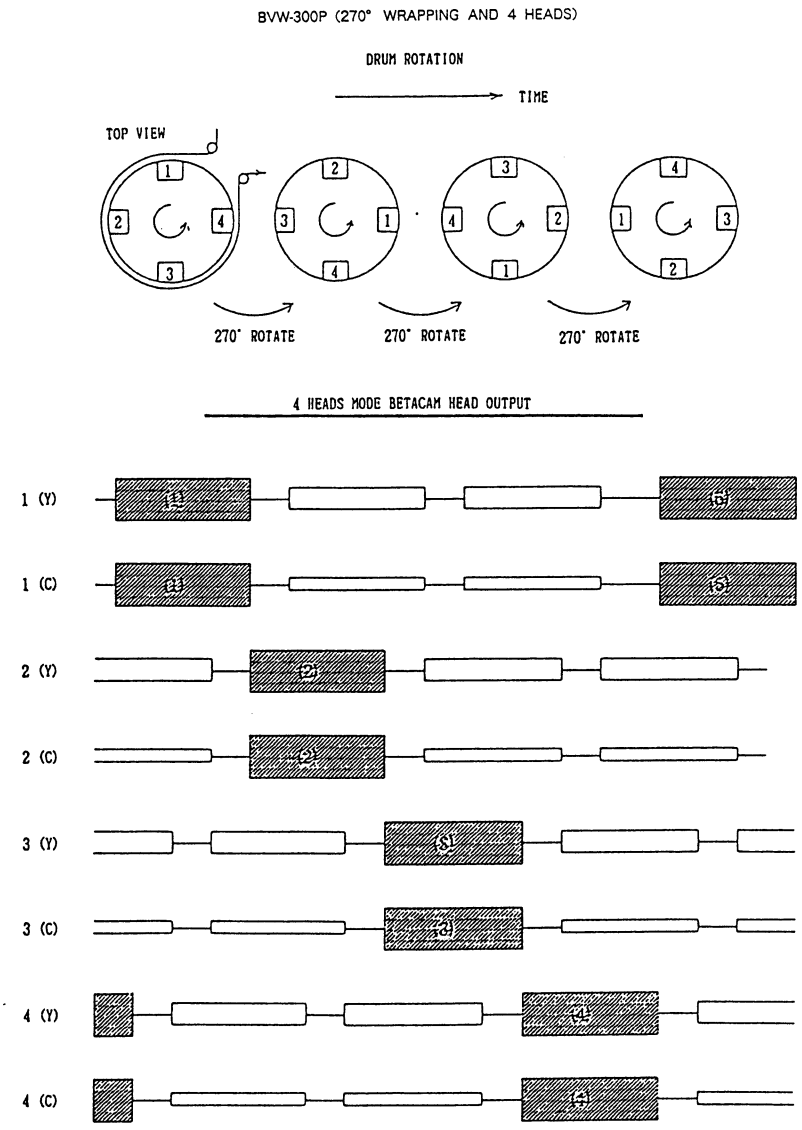
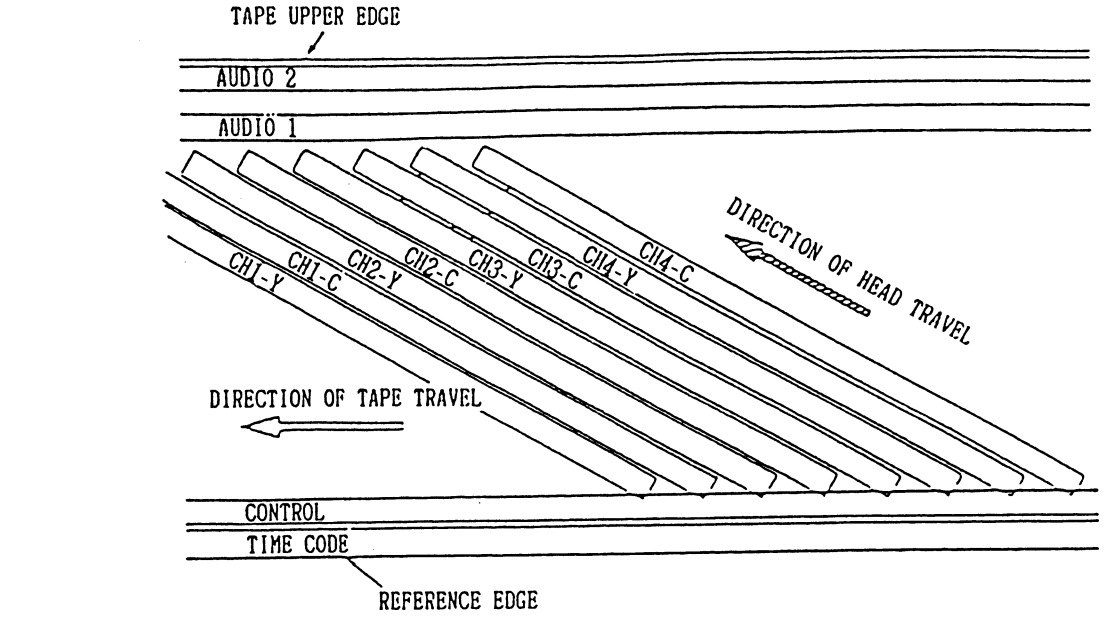



Fig. 1-3. Recording System



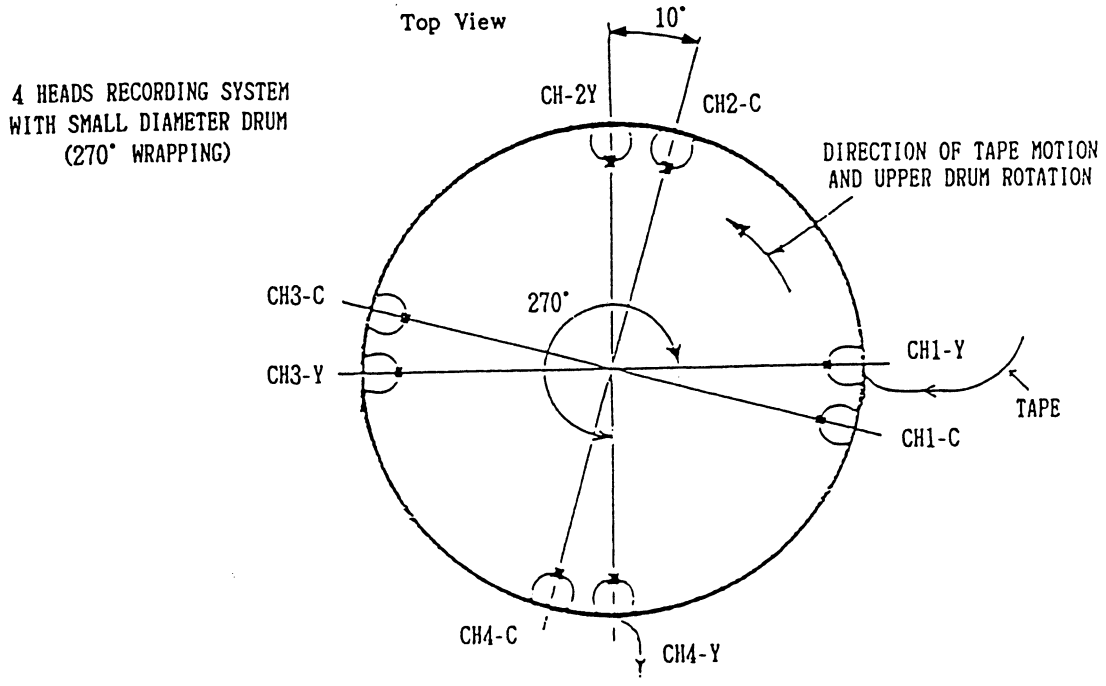




Fig. 1-4. Tape Pattern and Heads Allocation

## 1-3. REEL SYSTEM

The reel tables are driven by the capstan motor, timing belt and gear mechanism. The timing belt has the core-wire inside so that lift of the timing belt is more than three times of the conventional belt. The reel drive system has the following other features.

- Moving distance of the reel chassis is 15 mm.
- Threading time is approximately 2.5 seconds.
- Unthreading time is approximately 3.5 seconds.
- Gear reduction ratio from capstan to reel table is approximately 7.7.
- Capstan rotating speed to house the threaded tape (approximately 240 mm) into cassette inside is approximately 20 rotation at tape top and approximately 9 rotation at tape end. At this time approximately 10 g-cm soft brake is given on the supply reel table.

**[Variable Angle Gear]**
The gear is driven by the timing belt from capstan motor. Angle of this gear is made variable according to the rotating direction of capstan spindle, so that the tape is directed to the FWD or to the REW direction accordingly.

**[Supply/Take-up Idler Assembly]**
The S/T idler assembly is coupled with the gear to transmit the capstan motor torque. The S/T idler assembly has the magnet-clutch mechanism to that the T idler assembly is designed to have torque of 26±3 g-cm and the S idler assembly is designed to have torque of 113±9 g-cm.

**[Supply/Take-up Coupling Gear]**
In order to advance tape rapidly in FF/REW mode, more than 500 g-cm torque should be developed in the reel table. The S/T coupling gear functions to engage the magnet clutch mechanism of the S/T idler assembly. When an excessive winding torque happens, slip the gear in order to prevent the tape from damage. If any slip between the S/T gear and S/T idler should happen, the mechanism goes immediately into stop mode.

**[Brake ON/OFF Mode]**
The sub-soft-brake torque is approximately 3 g-cm, it suppresses the tape advance amount from the T reel in the back space edit mode. This sub-soft-brake give almost no effect on power consumption. The main brake is applied ON after capstan is stopped.

| REEL | MAIN BRAKE | SOFT BRAKE | SUB-SOFT BRAKE |
|---|---|---|---|
| S | STOP | FF/REW/STOP/ Loading/Unloading | None |
| T | STOP | FF/REW/STOP | Always ON |

**Table 1-1. Brake Operation**

| REEL | MAIN BRAKE | SOFT BRAKE | SUB-SOFT BRAKE |
|---|---|---|---|
| S | 80 g-cm | 10 g-cm | —— |
| T | 110 g-cm | 10 g-cm | 3 g-cm |

**Table 1-2. Brake Torque**

**[Cassette Sensors]**
The following five cassette sensors are equipped in this mechanism. The four sensors out of five for operating the shutter are installed in the reel chassis block and the remaining one sensor is installed in the cassette compartment.
The sensor-1 through sensor-4 starts functioning after tape threading is completed. The photo-sensor on the mother board is controlled to be ON/OFF by using shutter on the reel chassis block.

① Oxide recording inhibit
② Metal recording inhibit
③ Metal/oxide identification
④ Cassette-in switch
⑤ Cassette compartment lock switch

**[Tension Regulator]**
The tension regulator functions to control the tape tension at the drum entrance to be 23.5±3 g-cm (in the middle of tape).

## 1-4. CASSETTE COMPARTMENT

Cassette compartment consists of the both side frame, base cassette holder and various links.

**[Adaptation to the Moving Mechanism of the Reel Chassis]**

The cassette holder that is a part of cassette compartment assembly, has the slide mechanism that can travel 15 mm together with the reel chassis (see Fig. 1-5.). The slide mechanism is made possible by the bearing that supports the cassette holder's pivot in the longer slot of the cassette compartment.

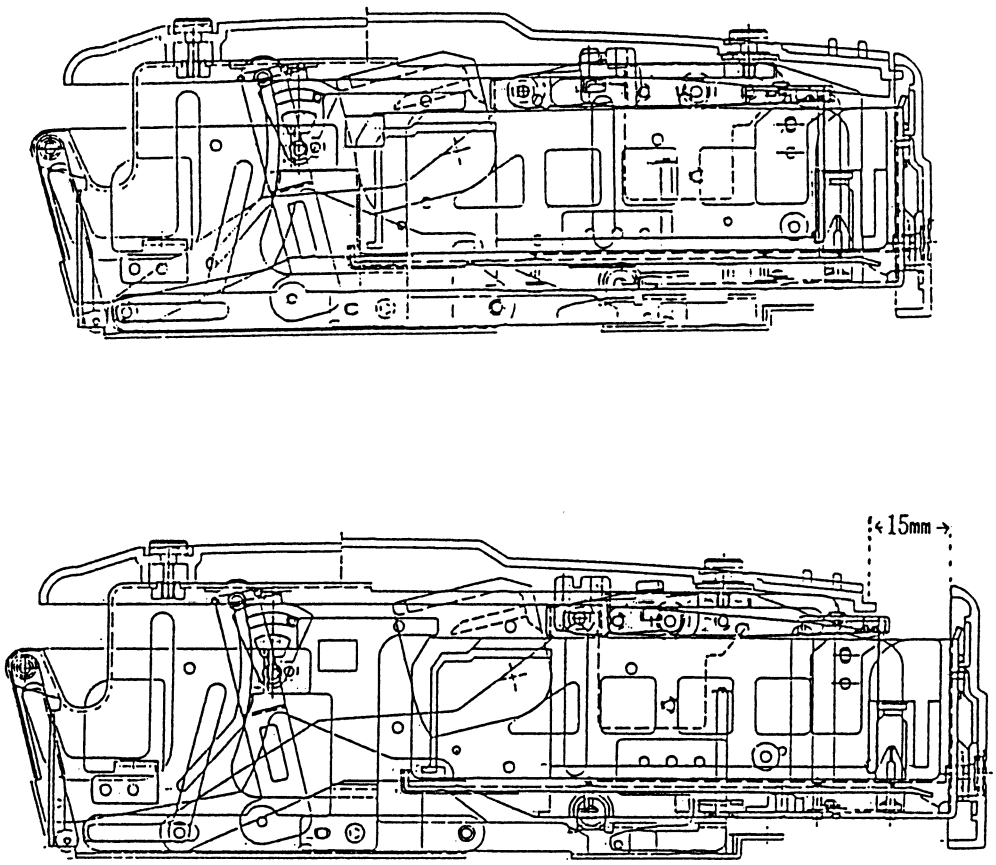



**Fig. 1-5. Slide Mechanism**

The cassette holder's pivot is lifted up (see Fig. 1-6) along with the L-shaped longer slot of the base by means of the "relay link" that moves with the pivot of frame, and by means of the "cassette compartment link" that moves with the pivot of base. By this mechanism, the cassette compartment can be opened approximately 20° . Opening of the cassette compartment is reduced by lifting the pivot. Also, the cassette holder is moved toward the cassette opening door by slanting the L-shaped slot so that the cassette can be easily taken out. Also, if the lock that fixes the relay links on both sides' frame, is unlocked, the cassette compartment can be opened as wide as approximately 75° (see Fig. 1-7.).

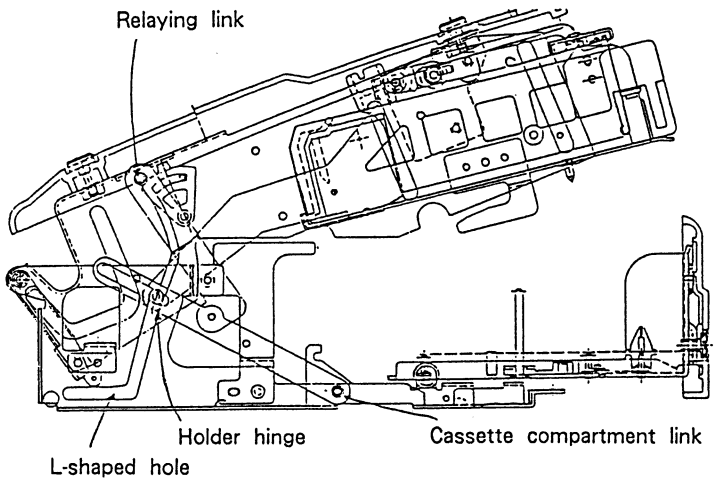



**Fig. 1-6. Cassette Compartment Open/Close Mechanism**

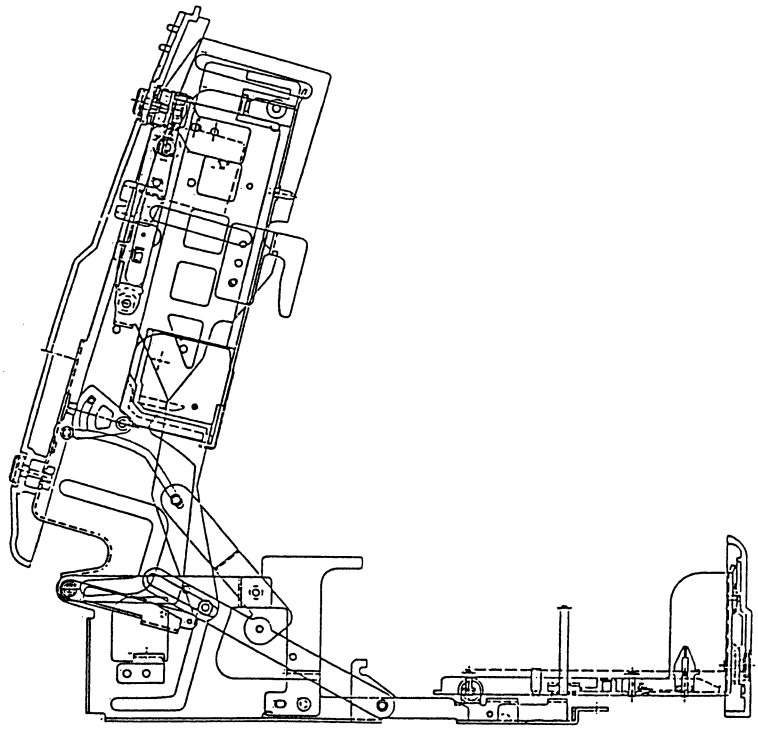


**Fig. 1-7. Mechanism Condition When Lock is Released.**

## 1-5. TAPE THREADING MECHANISM AND FUNCTION CAM

### 1-5-1. Structure

The threading ring drive, function selection and EJECT operation are done by one motor in this equipment. This mechanism consists of the following components.

- Function cam gear assembly
- Gear block assembly
- Threading motor assembly (including motor)
- Reel chassis driving slide plate

### 1-5-2. Outline of Mechanism

The threading ring is rotated by one motor in this mechanism. The braking operation and pinch on/off operation are controlled by the function cam in accordance with the requirement of each function modes.
Manual tape threading is possible in this mechanism. If cassette is ejected by manual operation, the lock mechanism is kept in the released state so that it is needed to turn the gear about half in the direction of loading in order to lock the cassette compartment again.

### 1-5-3. Function Cam Gear

Reel chassis and threading ring are driven by the rotation of the function cam gear.
Also the function gear drives the various mechanisms such as tension regulator, releasing the cassette compartment lock, soft brake, main brake, coupling gear and pinch roller pressing. It controls all the mechanical movement around 360° in corresponding to each modes of EJECT, FF, REW, STOP, PLAY and REC.

### 1-5-4. Intermittent Drive Mechanism

The intermittent drive mechanism is employed in the tape threading and in the function selection. During tape threading mode, gears of this mechanism are coupled to transmit power to drive the threading ring and reel chassis. After tape threading is completed and the function cam starts to operate, the power from the gear block is slipped by the shell portion of the intermittent gear so that transmission of power is inhibited. So the threading ring operation and reel chassis operation are prohibited.

### 1-5-5. Function Cam

The function cam operates for two purposes. One purpose is to drive the various mechanisms properly in each operating modes. The other purpose is to transmit its position to the system control circuit. For the purpose to drive the mechanism, the function cam has two grooves on the front surface and one groove in the back surface. The two grooves on the front surface are connected to the pinch/coupling gear/main brake/soft brake while the groove in the back surface is used to control the tension regulator ON/OFF and release the cassette compartment mechanically. Also, the label that is attached on back surface of function cam is used to read-out the positions of the four photo-sensors. The position detected signal of the four photo-sensors are coded into four bit data and became the gray code. The so called gray code is the code system where either one bit is changed when any one of modes is changed.

### 1-5-6. Other Mechanism

When tape is inserted, mechanism waits for next command input in the stop mode of operation.
When B0 code or B7 code is read-out, the tape slack is displayed on LCD through system control circuit, and the motor rotation is stopped.

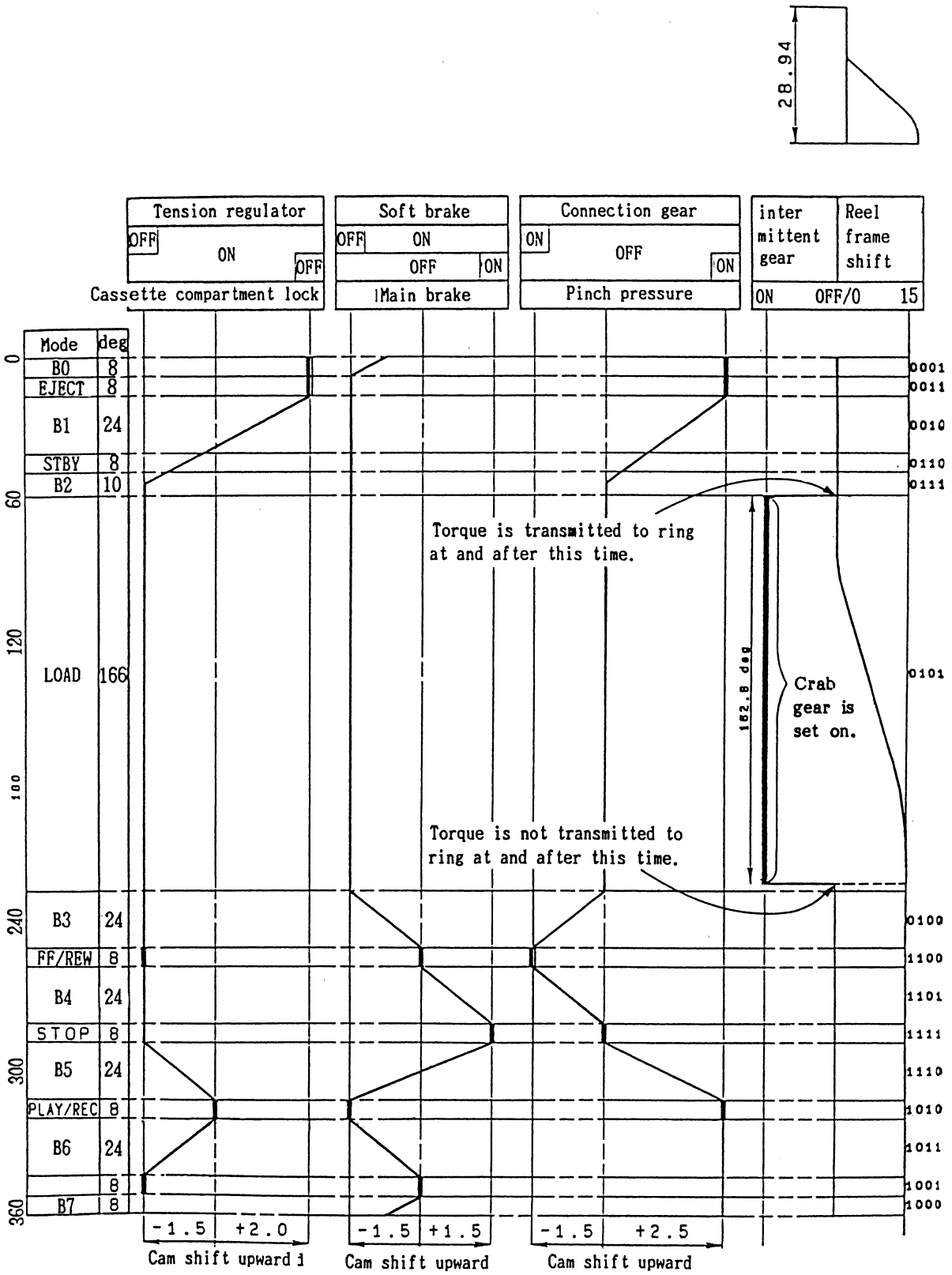



Fig. 1-8. Timing Chart

## 1-6. TAPE PATH SYSTEM

Tape path system is completed when the reel chassis is moved until the head drum is position inside the cassette. The head drum is positioned off-center of the cassette in order not to contact with the tape supporting portion in the center of cassette case. Capstan is placed in the position where it will not over-wrapped with head drum. The optimum positions of the full erase (FE) head, audio head and time code head are determined in relation with the drum and capstan positions. In order to make the mechanism small size, they are installed on the base chassis with no angle.

Tape run in this mechanism of this equipment, is determined mainly by the height of tape guides TG-5 and TG-7. Adjustment procedure for each stationary heads is same as that of conventional VTR. The CTL head requires height adjustment and position adjustment alone. The FE head requires no adjustment. Operation of the tape guides (TG) and impedance roller (IR) is described as follows.

- TG-1 : Limits upper and lower excursions of tape due to uneven winding of tape within a cassette.
- TG-2 : Functioning as a tension regulator
- IR-1 : Damps tape vibration (wow & flutter, jitter)
- FE : Erase head
- TG-4 : regulates the tape run with its lower flange
- CTL : Stationary CTL head
- TG-5 : Regulates the tape run at the drum entrance with the upper flange.
- IR-2 : Eliminates jitter that is generated by the FE head, CTL head and TG4/TG5, to prevent the adverse effect over drum.
- DRUM : Stabilizes tape run of its bottom edge with its rubbed edge.
- Slant guide : Changes the direction of tape run.
- TG-7 : Determines tape run at the drum exit with upper flange.
- TG-8 : Controls the tape run together with TG-7.
- Slant guide : Changes the direction of the tape run together with the neighboring slant guide.
- IR-3 : Removes the wow and flutter components and stabilizes the tape run along with the audio/TC heads.
- AU/TC & CONFI HEAD : REC/PB head of the audio/TC channel
- TG-10 : Presses tape with its upper flange, and controls the height of tape at the AU/TC and CONFI heads together with the lower flange of TG-8.
- CAPSTAN : Determines the tape speed.
- TG-11 : Prevents from irregular winding of tape.

The height of tape at the CTL head is determined by the lower flange of TG-4 and upper flange of TG-5. The height of tape at the audio head is determined by the lower flange of TG-8 and upper flange of TG-10.

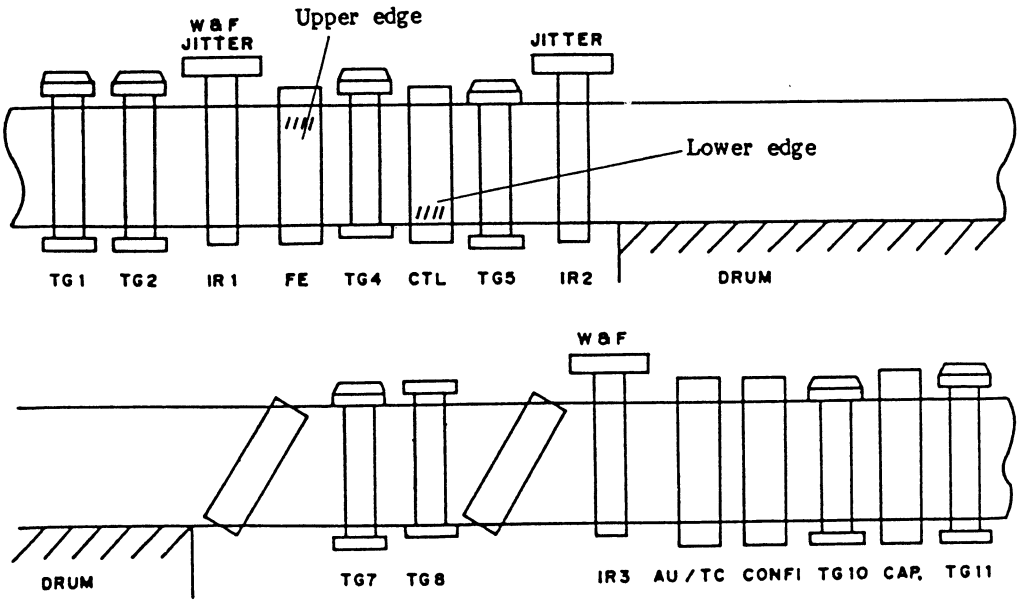



Fig. 1-9. Guides Positions

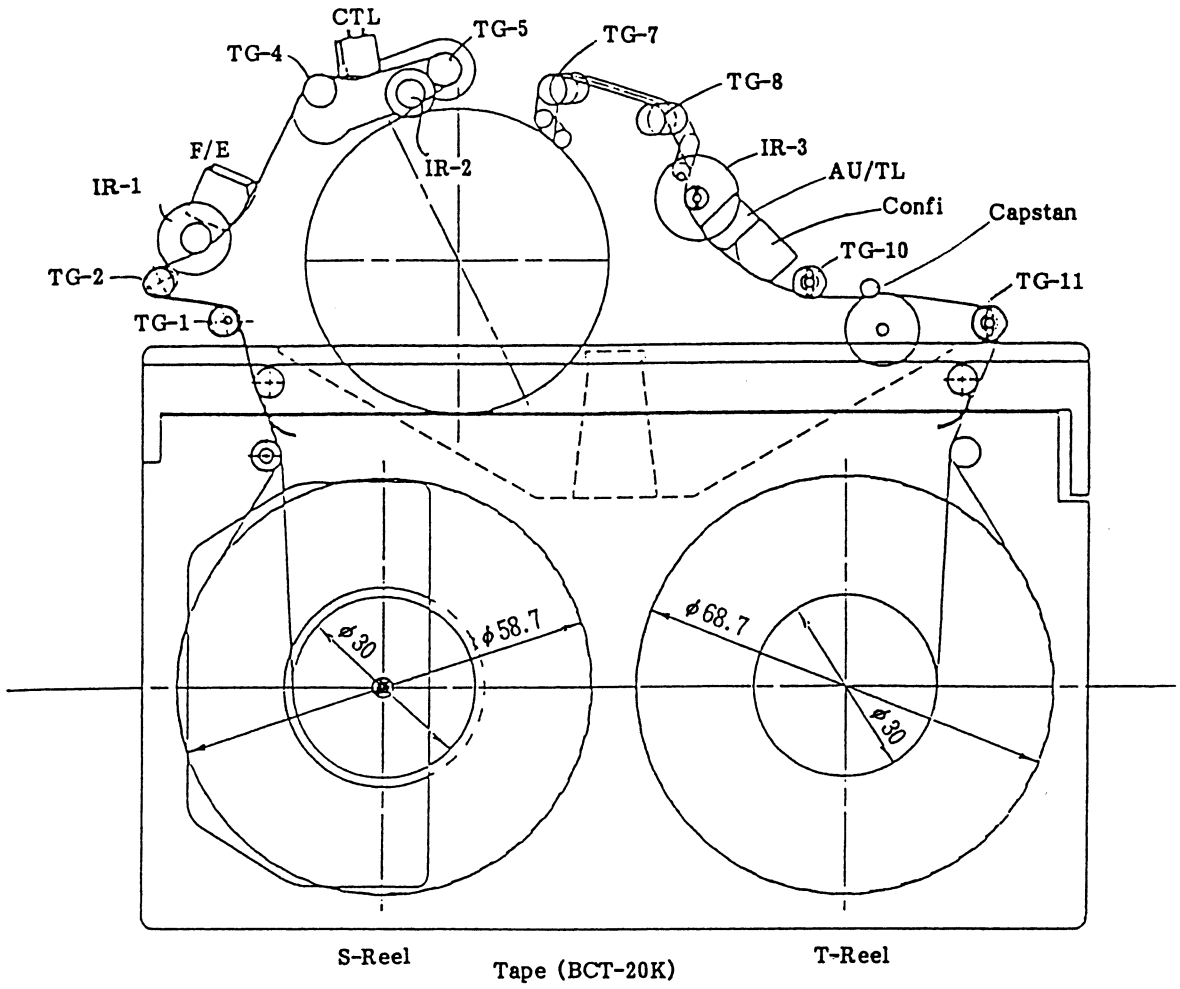



Fig. 1-10. Tape Path System

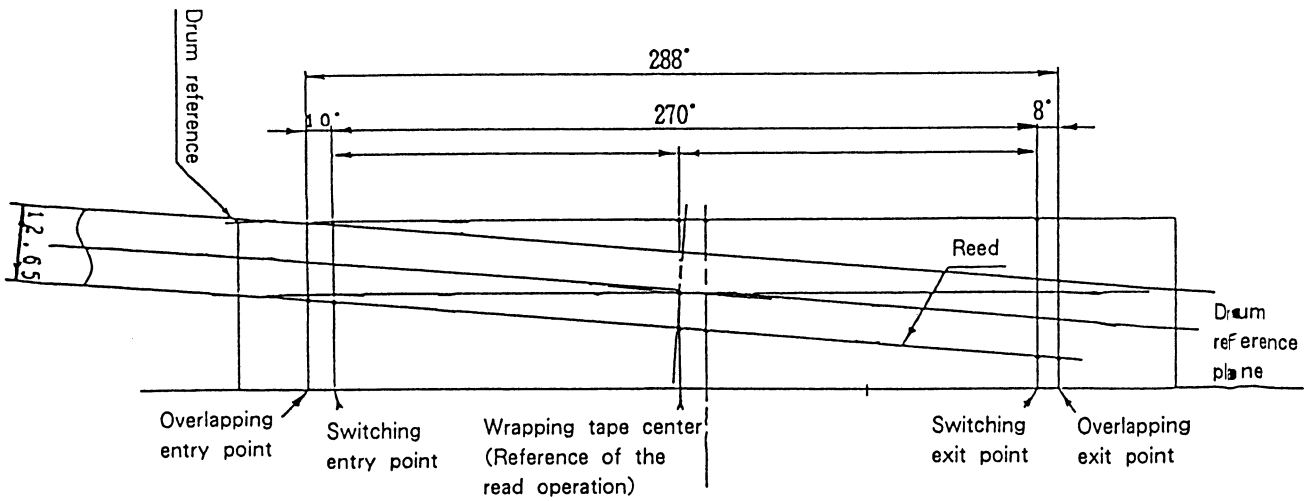



Fig. 1-11. Height of Each Points

## 1-7. TAPE THREADING

Tape threading mechanism pulls tape from inside the cassette, wraps it around the drum, and run the tape along with the stationary heads and each guides, as described below.

**[Tape Threading in the Supply Side]**

- As the extraction plate is pulled out together with threading ring rotation, the supply base is fixed into the V-ditch. So, tape is wrapped around the head drum.
- The IR-2 is brought closer to the head drum to prevent jitter from generation by each guide posts. The IR-2 is normally closed during threading.
- Tape guide TG-4 is opened just before completion of tape threading so that the tape is brought into contact with CTL head.

**[Tape Threading in the Take-up Side]**

- The T base is pulled out so that the tape is wrapped around the drum. As in the same manner as the supply base, the Take-up base is pulled toward the threading ring by the extraction plate. Just before completion of tape threading, the slant guide and TG-8 come down and are fixed by the lock plate.
  Tape is wrapped around the head drum with the slant guide positioned horizontally, the top of the guide TG-8 is pressed by the lock plate so that the guide should not jump due to abnormal tape tension during tape running.
  The take-up loading ring has one big gear that drives the big teeth on top of the take-up sub-cam so that the take-up sub-cam is rotated intermittently.

# SECTION 2
# VIDEO SIGNAL SYSTEM

## 2-1. FEATURES

This equipment has the following features.

- Compatible with SP format
- Four-head (Y/C : eight-head) configuration based on 270° wrapping system
- Simple playback function (Y and CTDM confirmations are possible through viewfinder.)
- Color playback is possible using playback adaptor.
- Simultaneous recording / RF alarm detection capability
- New ICs for smaller size, lighter weight and reduced power consumption
  SBX1523 (CTDM, timing pulse generator)
  SBX1524-01 (Y signal system : video processor, modulator)
  SBX1524 - 21 ( chroma signal system : video processor, modulator)
  SBX1491 (video REC/PB amplifier, timing pulse generator)
  CXD1357Q (timing decoder)

## 2-2. 4-HEAD 270° WRAPPING SYSTEM

The BVW-300P uses a small-diameter head drum to achieve its compact size and light weight. The smaller diameter of the head drum requires 270° tape wrapping the drum so that one field is recorded in just three-quarters of a revolution (270° ) of head drum. To maintain compatibility with the Betacam format, four sets of Y/C head pair are situated 90° apart from each other and the head pairs are switched on and off in sequence (Y1/C1 to Y2/C2 to Y3/C3 to Y4/C4) during recording and playback. It is necessary to perform head switching electronically inside the head drum between head paris in order to prevent interference between head paris because at least more than two head paris are in contact with the tape at any given instance. This head switching is performed by the switching circuit located inside the head drum.

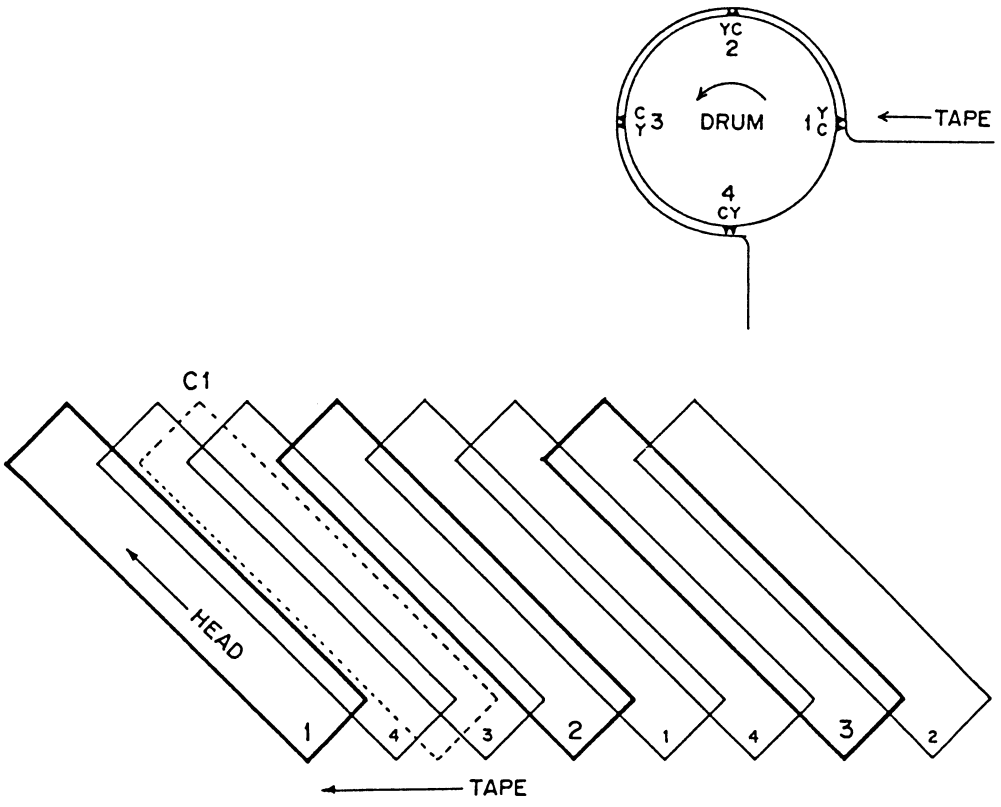



Fig. 2-1. 4-head 270° Wrapping System

## 2-3. VIDEO RECORDING SYSTEM

### 2-3-1. Chroma Time Base Compression Circuit (SBX1523)

The CTDM circuit is installed on the VDA-11 board. To make the circuit boards compact, major circuits use hybrid IC (SBX1523). The hybrid IC type SONY SBX1523 contains the following devices and peripheral circuits such as : CCDs (0.5H delay and 1H delay, each two), digital phase comparator, a timing IC (CXD1300A) a switching IC and peripheral circuits.

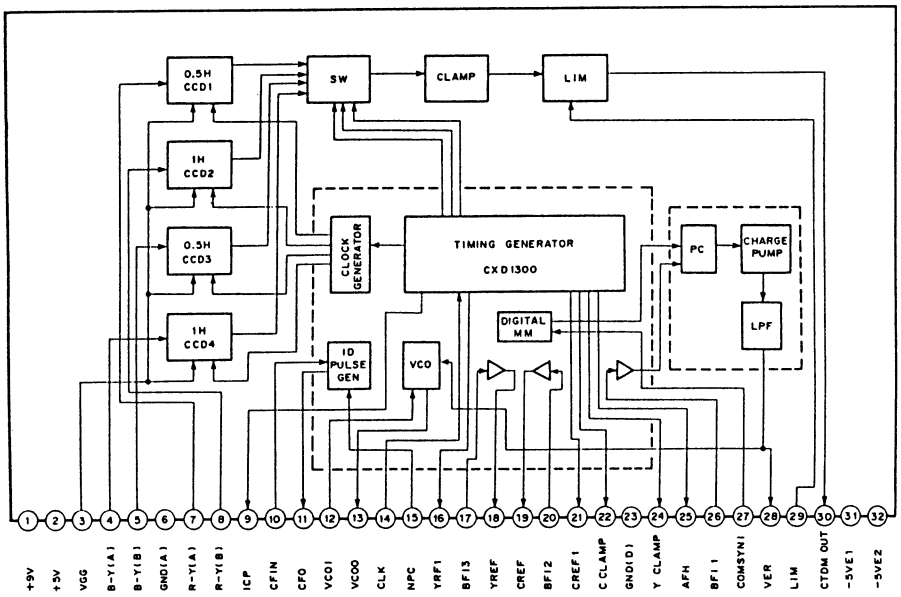



Fig. 2-2. SBX1523 Block Diagram

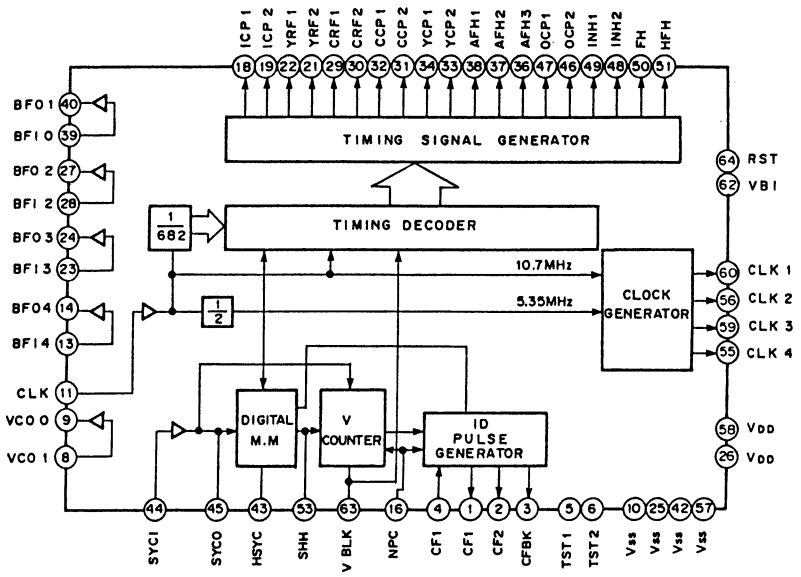



Fig. 2-3. CXD1300A Block Diagram

The color difference signals (R−Y, B−Y) that are supplied from the camera block receive amplitude adjustments by RV202, RV209, RV201 and RV210 in the VDA-11 board and are sent to pins 7, 8, 4 and 5 of IC201 (SBX1523). These color difference signals (R−Y, B−Y) are time-base compressed by the four CCDs that are located inside the IC and sent to switching circuits. The time-base compressed color difference signals are arranged in turn and become the CTDM signal. The CCD clock is generated by the IC (CXD1300A) inside IC201. The built-in IC CXD1300A generates the CCD clock, ID pulses and other various control signals too.

To prevent occurrence of CCD corner noise, the IC201 (SBX1523) uses the fixed pulse-width 5 MHz/10 MHz (40 nsec) and continuous clock systems as in the conventional VTR circuit. A CCD sync is added to the color difference signals before they are supplied to CCD input that enables the CCD to be operated at the optimum bias, simplified circuit and eliminated the need for bias adjustment. This CCD sync will be removed later in the hybrid IC (IC201) and will not be present in the output signal at pin 28 of IC201. The CTDM signal is passed through the clamp and limiter circuits located inside IC201 and is output from pin 28 of IC201. The clock components included in the CCD output signal is removed by the low-pass filter FL2. The CTDM signal is then input to an inverting amplifier consisting of Q3 and Q4 and is sent to pin 4 of IC2. The PLL circuit is consisted by the VCO, digital phase comparator, charge pump and active filter that are located inside CXD1300A.

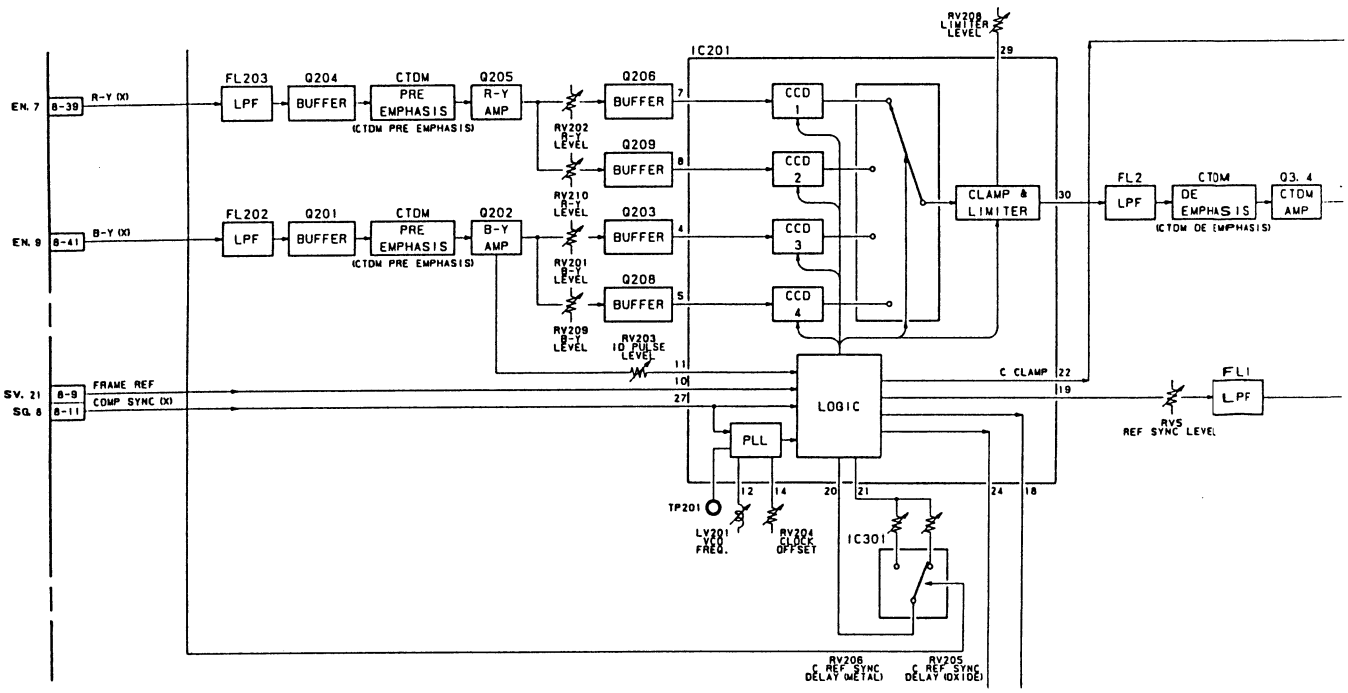



**Fig. 2-4. Chroma Time Base Compression Circuit**

### 2-3-2. Video Signal Processing

The Y and C signals use the IC type SBX1524 video processor. The Y signal processing uses the AFM board IC1 (SBX1524-01). The C signal processing uses the VDA-11 board IC2 (SBX1524-21). Because Y signal circuit and C signal circuit are identical, explanation is given to the C signal circuit only. The CTDM signal input from pin 4 of IC2 on the VDA-11 board is mixed with the reference sync signal of pin 1 of IC2 and sent to an inverting amplifier. In the case of Y signal, a VITC signal is mixed together with the reference sync signal. The sync-added CTDM signal is sent to the non-linear preemphasis circuit and preemphasis circuit that are located inside IC2. The CTDM signal is then frequency modulated.

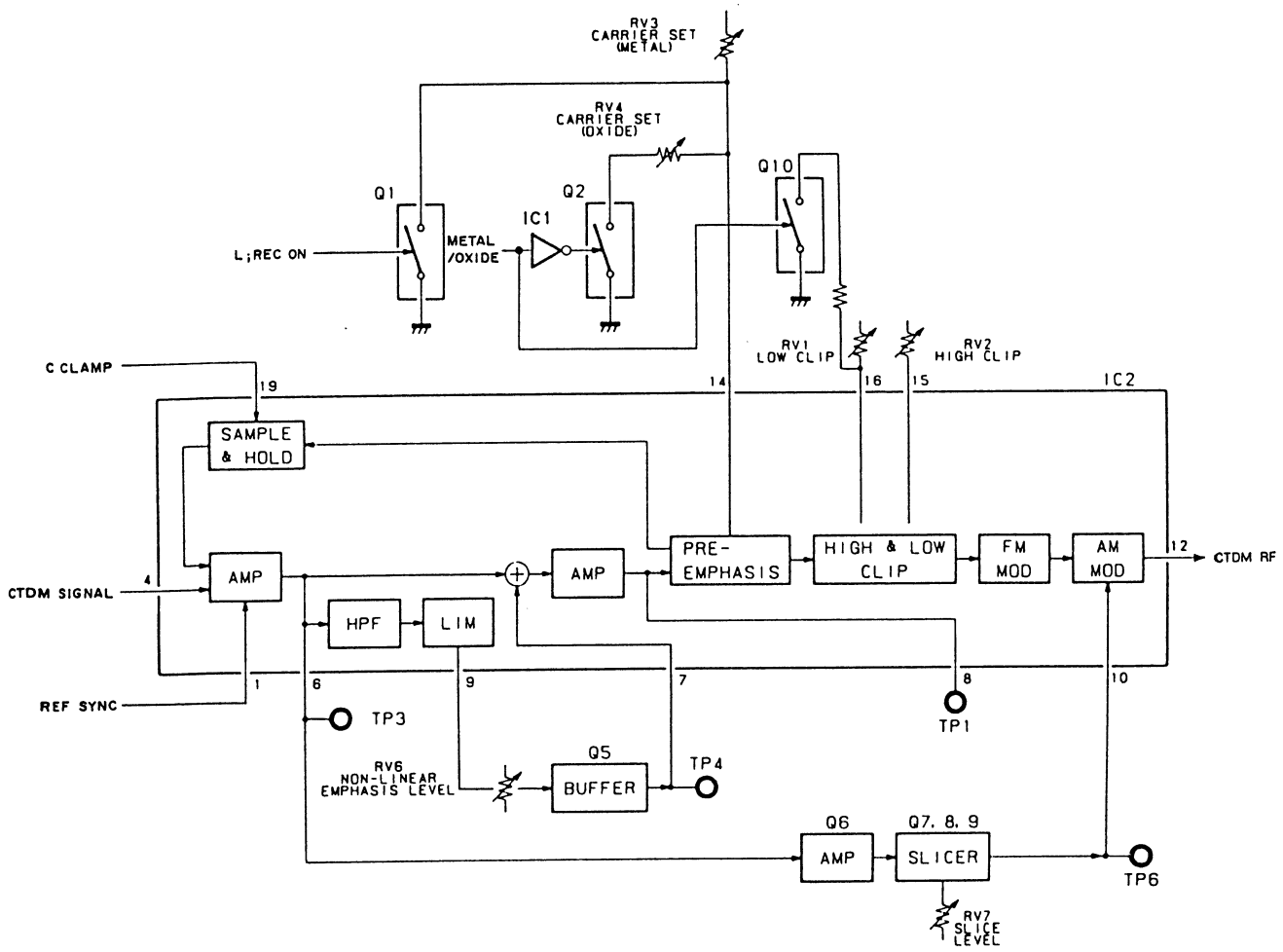



Fig. 2-5. Video Signal Process Circuit and Peripheral Circuit

### 2-3-3. Nonlinear Preemphasis Circuit

The CTDM output signal from the inverting amplifier passes through a high-pass filter consisting of capacitor and resistor, and is sent to a limiter. The limiter output is sent out from pin 9 of IC2. The nonlinear preemphasis signal level is adjusted by RV6, buffered by Q5 and again sent to pin 7 of IC2 and then to inverting amplifier. The main CTDM signal is mixed with the nonlinear preemphasis signal that has received the level adjusted, at the 2nd inverting amplifier.

### 2-3-4. Preemphasis and Clip Circuit

The CTDM signal level is reduced to approximately 1/3 of the input CTDM signal. The CTDM signal is sent to the pre-emphasis circuit where the linear emphasis is applied to the signal. The time constant of this preemphasis is determined by a CR in the hybrid IC2. The level clamping is done by the clamp pulse input to pin 19 of IC2. The emphasized CTDM signal is again sent to level-clip circuit. The high-clip level (white clip in Y signal) is adjusted by the pin 15 of IC2 dc voltages with RV2. The low-clip (dark clip in the Y signal is adjusted by pin 16 of IC2 dc voltage with RV1. Q12 is the metal/oxide select switch during the low-clip mode.

### 2-3-5. FM Modulator

The CTDM signal after pre-emphasis and clipping is V-I converted and then frequency modulated. Deviation can be adjusted by RV1 on the IC2 (SBX1524). The carrier frequency for metal is determined by the current flowing in pin 14 of IC2 by means of adjustments RV3 and R5. The carrier for oxide tape is adjusted by dividing the current that was set by RV3 and R5, further by using RV4 and R6.
When equipment is not recording, Q1 is ON, stopping record current from flowing to pin 14 of IC2 and oscillation of the carrier stops. The carrier balance is adjusted by RV2 on the IC2 that minimizes the secondary distortion of the output CTDM RF signal. The frequency modulated CTDM signal is sent to am modulator.

### 2-3-6. Nonlinear FM Carrier Enhancer

This circuit consists of an AM modulator that minimizes the overmodulation. The CTDM RF output signal from pin 6 of IC2 is tuned by C11 and L4. The phase inverted CTDM RF signal is inverted, and sent to a slicer consisting of Q7, Q8 and Q9. The slicer circuit extracts the high-amplitude components only in the range of 2.3-to-4 MHz from the CTDM RF signal. The slice level can be adjusted by RV7. The CTDM RF signal is amplitude modulated by the signal extracted by the slicer. The portion of the recording current that is extracted by slicer is amplified so that the overmodulation is suppressed. There is a tendency that the carrier leak happens when signal level change is significant and signal rise-up is steep (frequency response is high). So, only these signal portions are emphasized for larger record current in order to prevent the carrier leak.

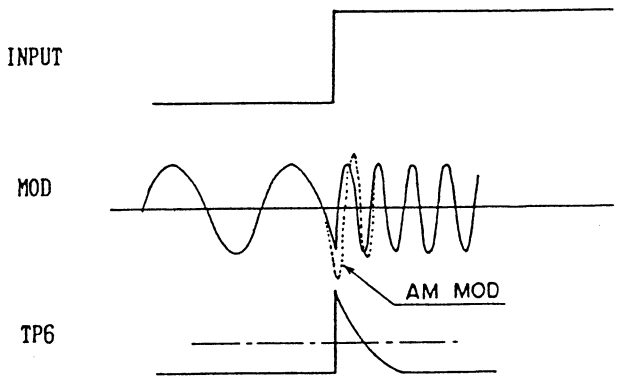



Fig. 2-6. Non-linear FM Carrier Enhancer

### 2-3-7. AFM Mixer (C Signal System Only)

The RF signal output from IC2 is passed through the RF equalizer and AFM trap circuit consisting of an LCR (only in metal mode) and then input to the AFM mixer. In the two-head (180-degree wound) type VTRs such as the BVW-75P, if there is a difference in amplitude during playback between two channels, A and B, the playback RF signal will have two types of level difference as shown in Fig. 2-7.

If a tape recorded on the BVW-300P is played back on the BVW-75P, the A channel playback will have two different RF level difference because the A channel will playback either ① or ③ as shown in Fig. 2-8. The B channel playback will have two different RF level difference as it will playback either ② or ④. These level difference can be compensated by using record equalizer, but the AFM signal cannot be compensated by record equalizer since AFM signal uses very low frequency against the video frequency band-width.

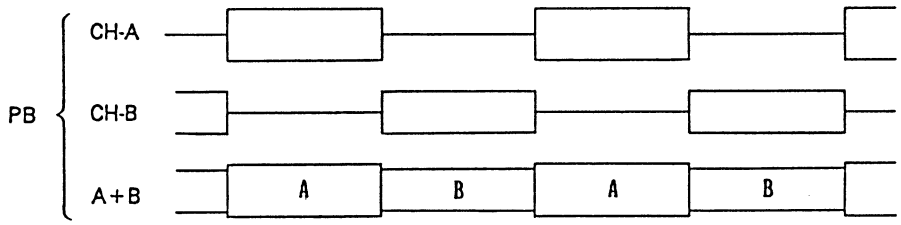



Fig. 2-7.

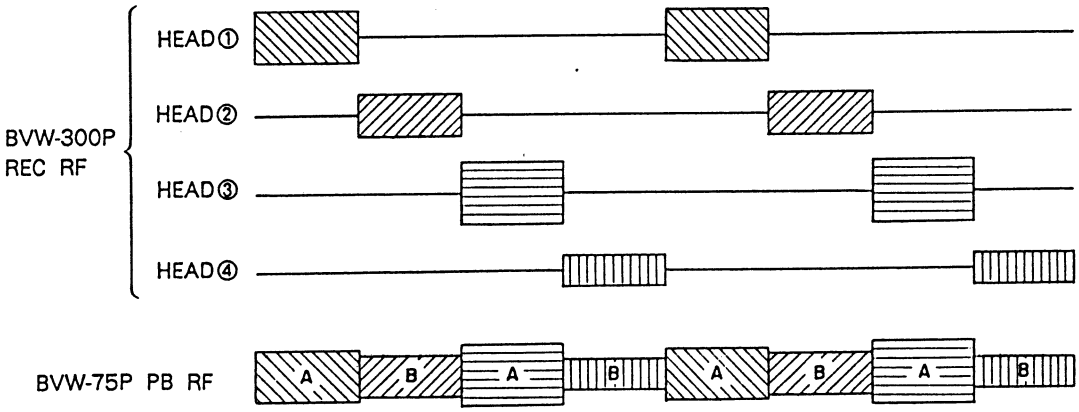



Fig. 2-8.

Therefore, in order to reduce level difference between channels as small as possible, AFM recording level among channel is adjusted.
The AFM carriers (310 kHz and 540 kHz) are supplied from the AFM-6 board is passed through a low-pass filter and multiplexed with CTDM RF signal, and are sent to rotary transformer. The recording channel balance between CH-3 and CH-4 is adjusted by RV108 using the CH-4 switching pulse.

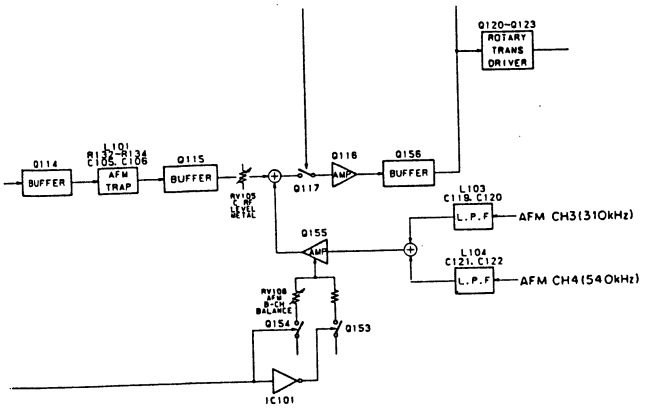



Fig. 2-9.

## 2-3-8. REC Equalizer

In the BVW-300P, a REC/PB amplifier is built inside the head drum. Therefore, the record current and frequency response characteristics cannot be adjusted in the record amplifier unlike other models. This means that these adjustments must be performed in the former stage of the record amplifier.
The record equalizer circuit primarily consists of FET switchers (Q108 through Q111 and Q158 through Q161) plus a CR. The record switching is synchronized with the head switching pulse sent from the VP-24 board. For example, when recording is done in head-1, Q108 and Q158 are turned on and the characteristics set by CV1 and RV101 is selected. After frequency response and gain adjustment, the RF signal is sent to the record amplifier in the head drum via a buffer amplifier.

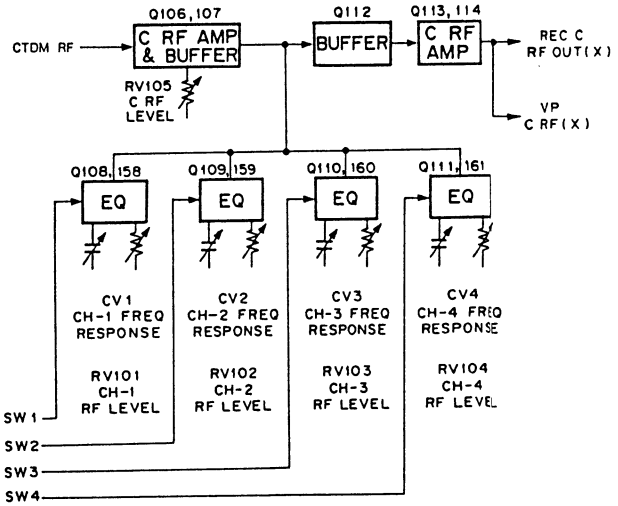



Fig. 2-10. Record Equalizer (chroma signal system)

### 2-3-9. Record/Playback Amplifier

The record/playback amplifier and timing decoder for controlling each amplifier are incorporated on a hybrid IC (SBX1491).

- CXA1222 (REC amplifier) : 8pcs
- CXA1077 (PB amplifier) : 4pcs
- CXD1327 (Timing decoder) : 1pcs

The record Y RF signal that is supplied from the rotary transformer is input to pins 2 and 13 of Y recording amplifier IC2 (CXA1222) with differential level. One side of the record C signal is grounded, and the other side is sent to pins 2 and 13 of recording amplifier.

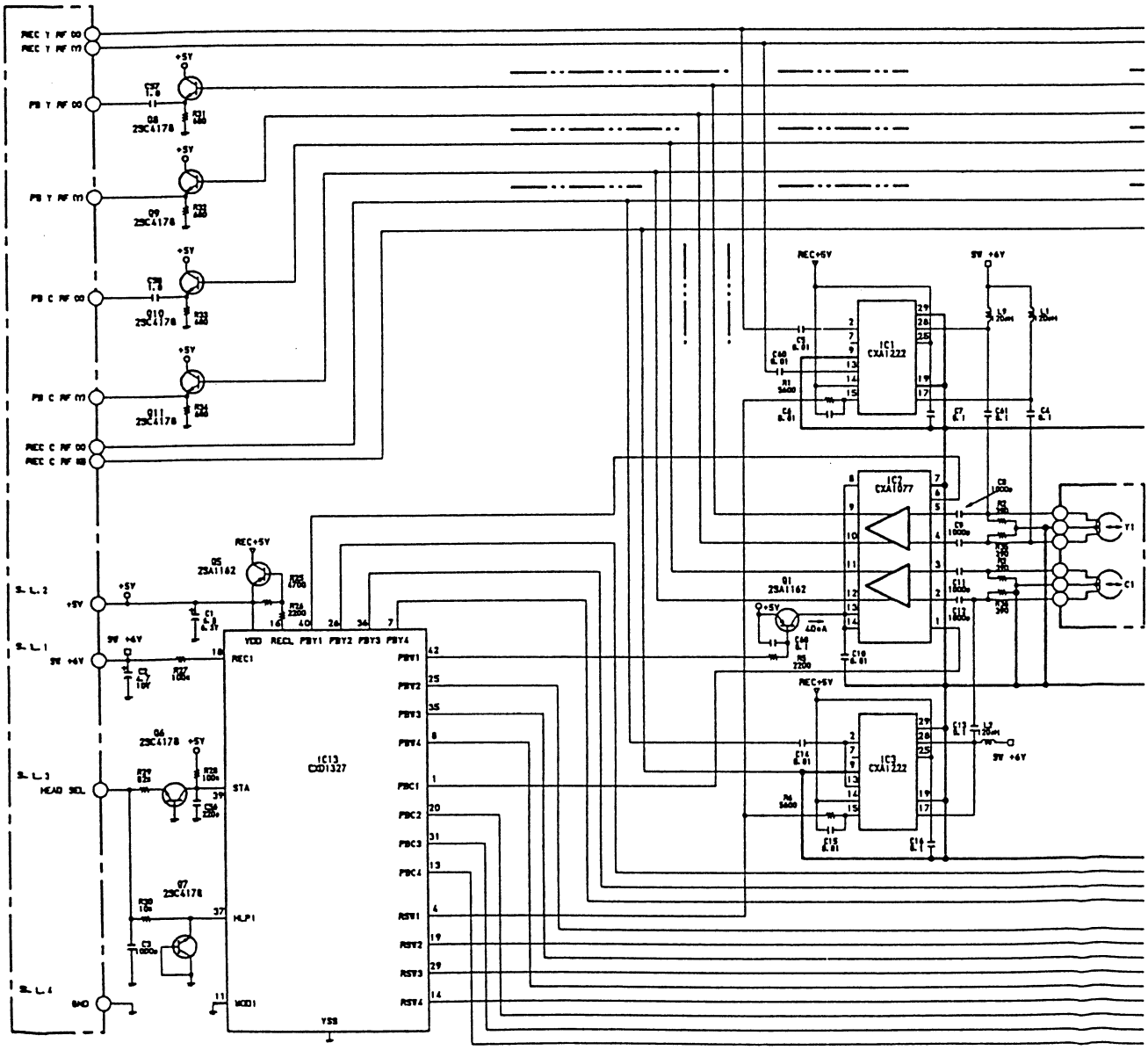


Fig. 2-11. Record/Playback Amplifier

### 2-3-10. Center Tap Video Head

Since the video head winding is equipped with a center tap, however, only half of the total windng is used for recording in C system and remaining winding is used for playback only.

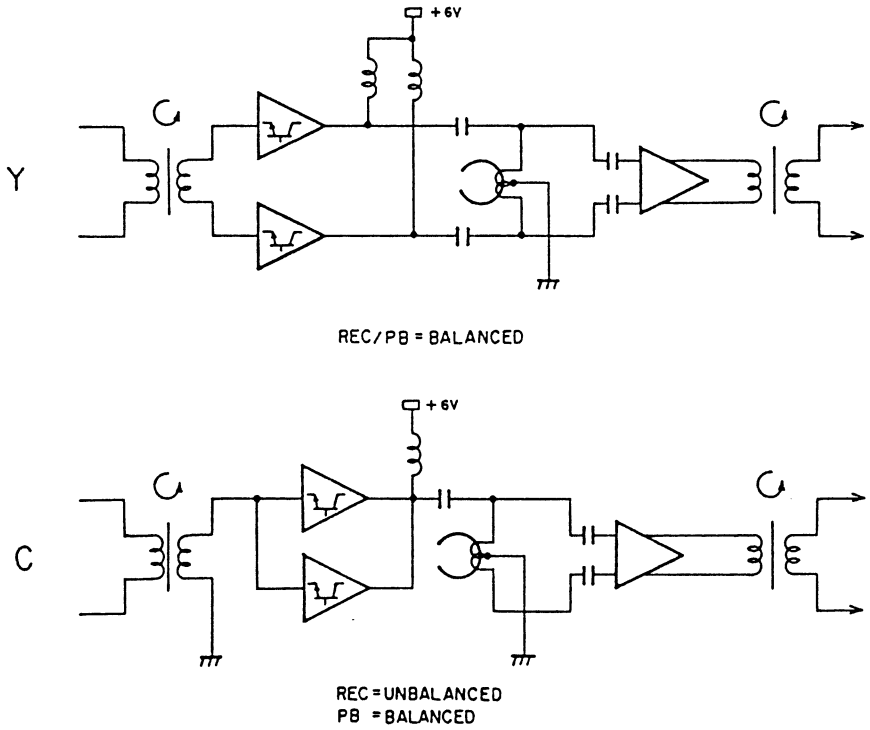



Fig. 2-12. Center Tap Video Head

## 2-3-11. Record/Playback Control Timing

A set of recording amplifier and playback amplifier are connected to each head in this equipment. The proper head is selected by the control signal that is supplied from outside control circuit. In order to switch the control signals in synchronism with head drum rotation, the correct switching timings should be supplied from external circuits. So, this equipment uses the following control method.

The timing pulse that is generated by the servo microcomputer on the SV-97 board is converted to the tri-state logical signal in the VP-24 board, and is sent to the record/playback amplifier (SBX1491) through a slip-ring (one stack of slip rings). This pulse is decoded by the gate array IC13 (CDX1327) that is housed inside SBX1491, and all the control signals are obtained.

In order to reduce power consumption during recording, the switchers Q1, Q2, Q3 and Q4 are turned off during recording so that it cuts off power to the playback amplifier. However, these switchers are turned on during the RF alarm signal detection timing. Also, because the protection diode in the playback amplifier input absorbs the recording current, power is supplied to the currently recording channel only in order prevent the record current absorption.

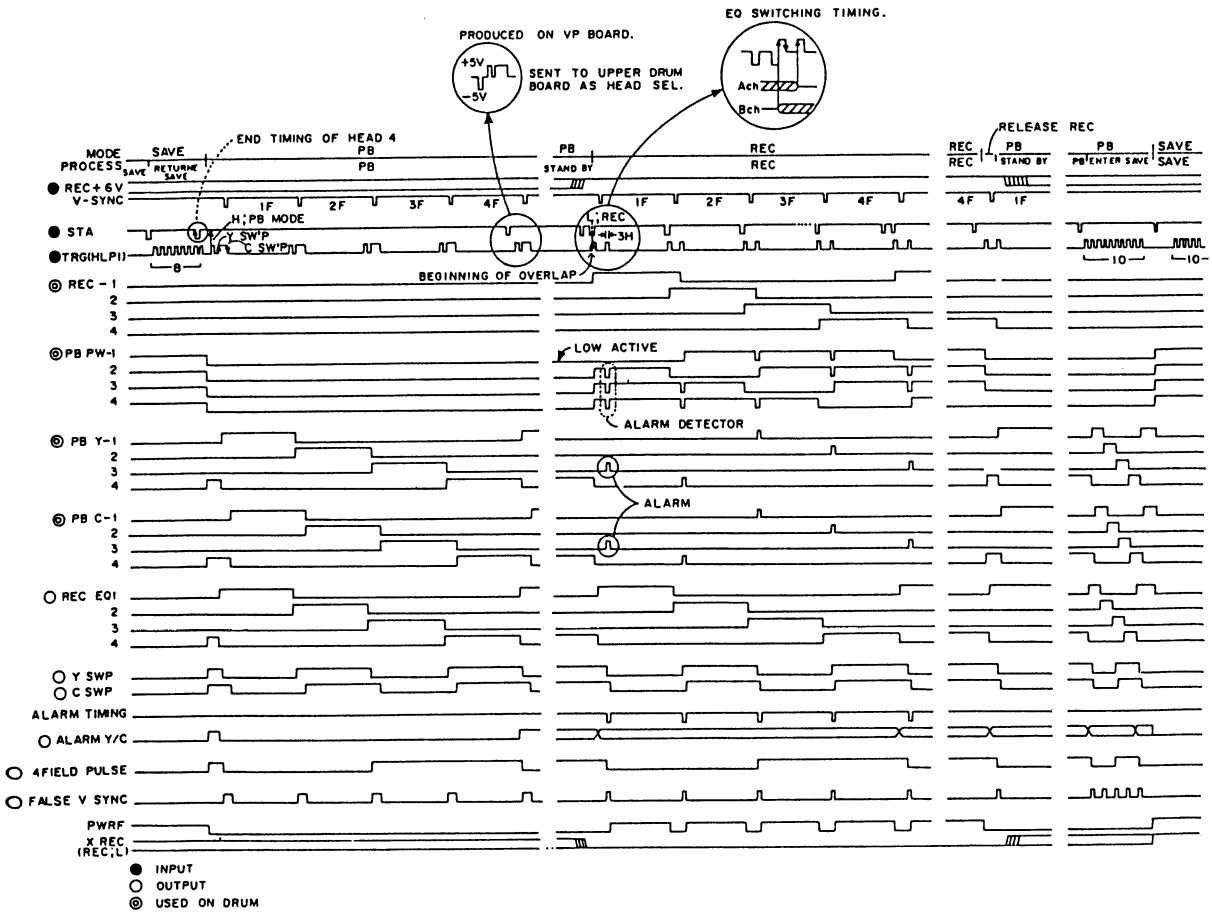



Fig. 2-13. Record/Playback Control Timing

## 2-4. VIDEO SIGNAL PLAYBACK SYSTEM

The playback system is incorporated on the VP-24 board and performs the following functions :

- Interface for the playback adaptor
- Demodulation for simple playback on viewfinder
- Record RF alarm detection
- Record/playback timing pulse generation

### 2-4-1. Playback Adaptor Interface

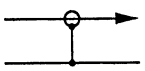
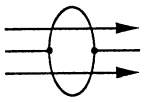
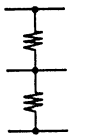
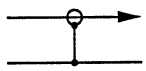
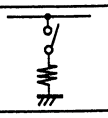
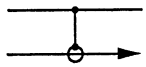
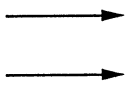
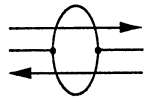
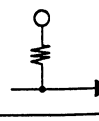
| PIN NO. | DESCRIPTION | VTR SIDE | DIRECTION | PB ADAPTOR SIDE |
|---|---|---|---|---|
| 1<br>2 | Y.RF (X)<br>(G) | 0.2 Vp-p±0.01 Vp-p (METAL)<br>Variation among channels : ±20mV or less<br>Center carrier : ±5kHz or less<br>75 Ω DC=0V |  | <br>75 Ω |
| 3<br>4<br>5 | LNG AUDIO CH 1 PB (X)<br>(G)<br>LNG AUDIO CH 2 PB (X) | LOW IMPEDANCE<br>−10 dBu±0.2 dB |  |  <br>10 kΩ or more<br>10 kΩ or more |
| 6 | METAL "H" | METAL : +5V<br>FF.REW : +2.5V<br>OXIDE : 0V |  | Active High |
| 7<br>8 | GND<br>GND | |  | |
| 9<br>10 | ENCODE VIDEO (X)<br>(G) | 1 Vp-p composite video with 75 Ω termination |  |  <br>75 Ω |
| 11<br>12 | (BVW-300P) (G)<br>C.SWP<br>(BVV-5PS) (X)<br>C (B) RF | (BVW-300P) A : H<br>0.3V B : L<br>(BVV-5PS)<br>Same as Y RF |  | <br>75 Ω |
| 13<br>14 | +12V<br>+12V | Output directly from battery or EXT DC. |  | |
| 16<br>15<br>18 | Y RF SW PULSE (X)<br>(G)<br>ADV SYNC (X) | Open collector<br>A : H<br>B : L<br>75 Ω |  |  <br>5V<br>10k<br>2±0.5V |
| 17 | PLAY "H" | BVW-300P: 9V<br>BVV-5PS : 5V<br>10k |  | Active High |
| 19<br>20 | C (A) RF (G)<br>(X) | Same as Y RF | | <br>75 Ω |

**Table 2-1. 20P Multi-Connector I/O Specifications**

### 2-4-2. Y/C RF Switching Pulse Output Circuit

According to the specifications of the playback adaptor, polarity of the switching pulse is High for channel A and Low for channel B.

#### (1) Y RF switching pulse output circuit

Because Q26 is used in an open collector connection, this signal is pulled up (+5V/10 kΩ) in the playback adaptor circuits.

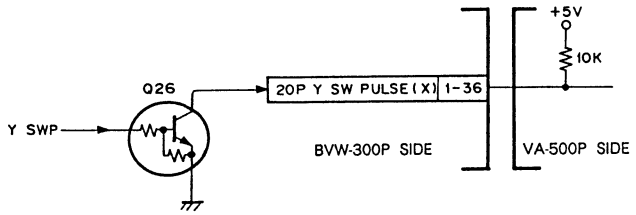



Fig. 2-14. Y RF Switching Pulse Output Circuit

#### (2) CRF switching pulse output circuit

Because the chroma channel RF signal is terminated by 75 Ω with playback adaptor, Q25 is used in open emitter connection. The series resistor (R92 : 1 kΩ) is inserted to reduce the power consumption.

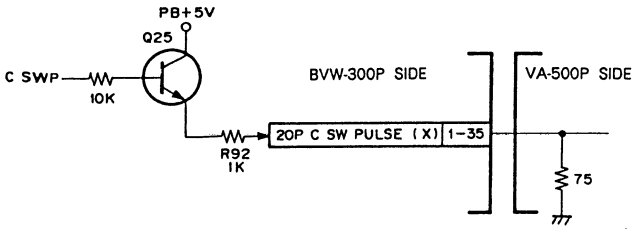



Fig. 2-15. C RF Switching Pulse Output Circuit

### 2-4-3. Playback Adaptor Control Signal Generator

The METAL/OXIDE sensing signal and FF/REW information are supplied from the system control circuit and sent to IC6 and Q30 that produce the FF/REW signal and other signals.

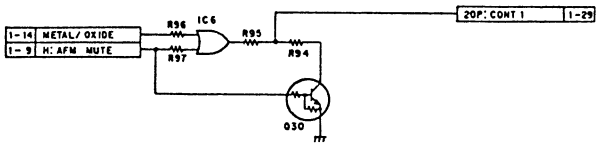



Fig. 2-16. Playback Adaptor Control Signal Generator

### 2-4-4. Encoder Power Save Circuit

The power save switch is equipped in the VIDEO OUT BNC connectors on the side and rear panels of the unit. When a BNC cable is connected and is detected by the detector, the encoder circuit is designed to start its operation in order to save the power. However, since no connecting switch is adopted in the 20P connector, Y switching pulse is detected as follows.

The Y switching pulse that is supplied from playback adaptor, is pulled up in the playback adaptor circuit. During the Y switching pulse is Low level, the power save sensing circuit cannot detect the BNC cable connection. So, the signal level detected by C83 is kept held to make the detection possible. The detector consists of Q27, Q28 and Q29. When Q29 is turned on (short-circuited condition), the power to the encoder is connected to on.

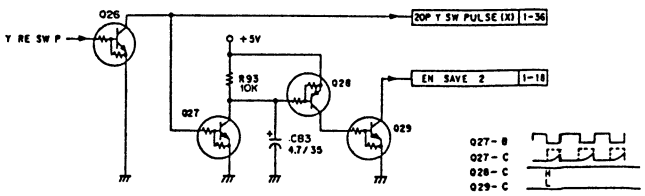



Fig. 2-17. Encoder Power Save Circuit

## 2-4-5. Playback RF Circuit

The Y RF signal is input from pins 41 and 42 of CN1 and the C RF signal is input from pins 44 and 45 of CN1. After passing through a high-pass filter consisting of a CR, the Y RF signal is sent to the RF amplifiers IC1 and the C RF signal to IC2. The 100 pF capacitors (Y : C20 and C : C50) in the input circuits of these ICs are for matching the RF frequency response with that of BVV-5PS. The Y RF signal gain is adjusted by RV21, RV23, RV25 and RV27, and the C RF signal gain by RV51, RV53, RV55 and RV57. The Y RF signal is sent to a low-pass filter consisting of Q12, Q13 and LCR, and the C RF signal to that consisting of Q19, Q20 and LCR. This low-pass filter is used for eliminating the noise of more then 14 MHz.

After passing through the low-pass filters, the PB Y RF and PB C RF signals are passed through buffers Q14 and Q21, respectively, before being output via the 20P connector (playback adaptor).

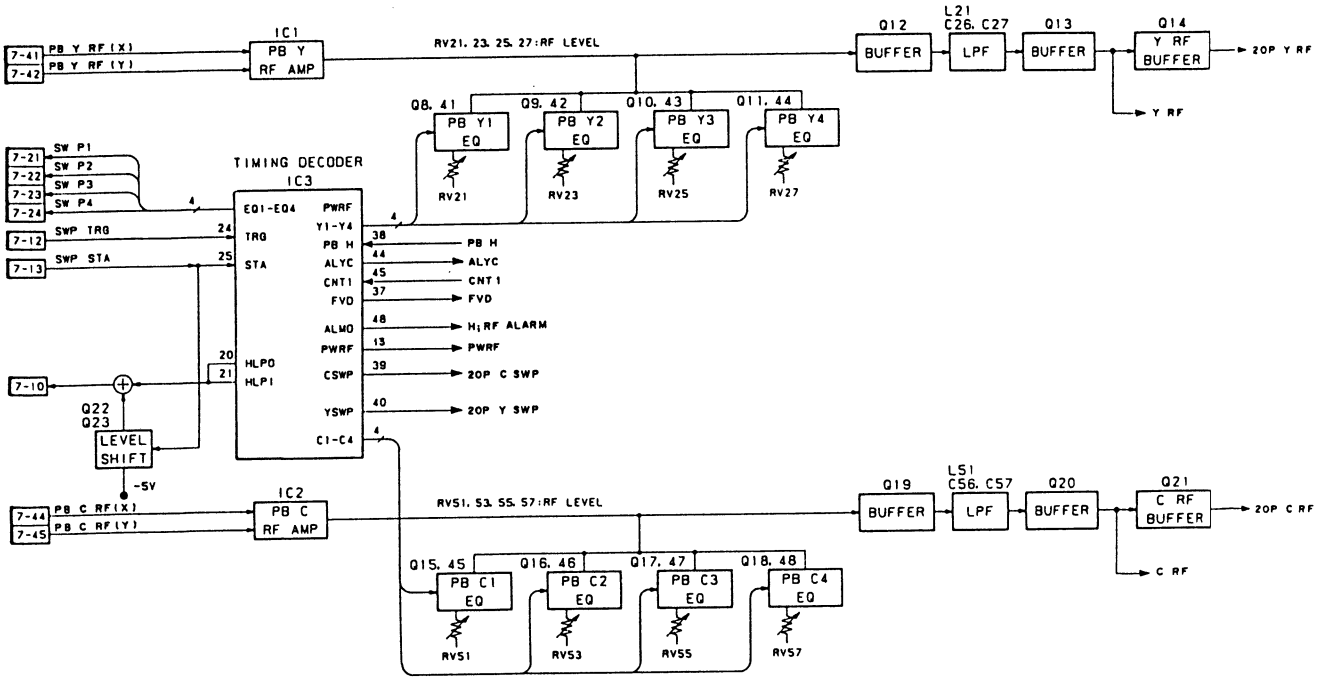



Fig. 2-18. Playback RF Circuit

### 2-4-6. FM Demodulator for the Viewfinder

The playback Y RF and C RF signals are sent to the switcher IC4 (2/4) where either one of the two signals is selected and feeds to pin 14 of IC4. The selected signal is sent to a peaking circuit consisting of Q31 and Q32 and LCR, in order to prevent the carrier leakage phenomena.

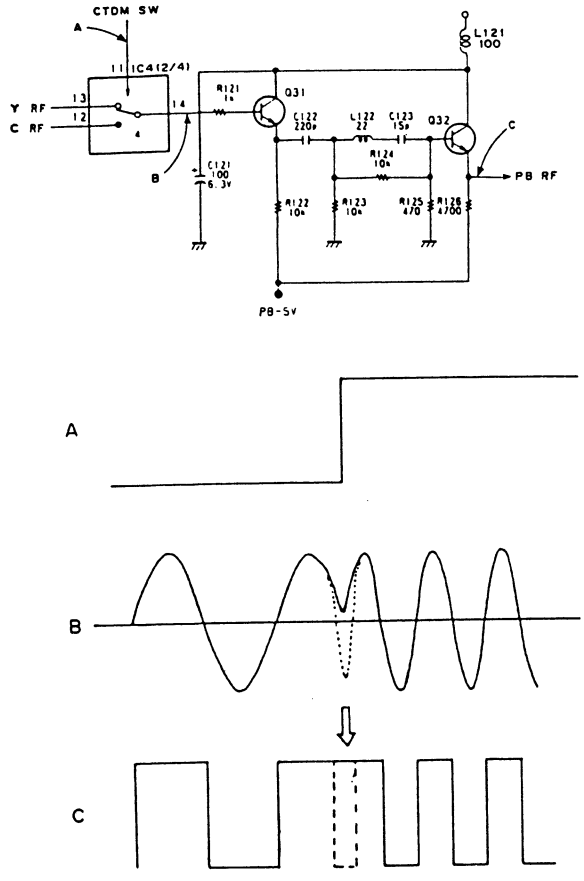



Fig. 2-19. Peaking Circuit

The playback RF signals after the peaking circuit is then sent to pin 48 of IC5 where it is passed through the AGC circuit that is incorporated inside IC5 and is sent to the demodulation circuit. R141 and C142 provide the AGC time constant. R142 is also the resistor which sets the time constant for the monostable multivibrator of the frequency-to-voltage (F/V) conversion. The demodulated signal is output via pin 12 of IC5. After carrier components are removed from the signal by a low-pass filter consisting of L123, C124 and C125, it is input to the buffer Q33. This transistor acts as a buffer for Y and as an inverter for C. This is because the chroma signal system (CTDM signal) sync has positive polarity. The Y signal after Q33 is sent to pin 3 of IC4 (4/4). The
chroma signal after buffer Q34 is sent to pin 5 of IC4 (4/4). Since the IC4 (4/4) is a switcher IC, either Y signal or chroma signal selected by IC4 is obtained from pin 4 of IC4 and sent to pin 40 of IC5 where the selected signal is sent to the de-emphasis circuit inside IC5.

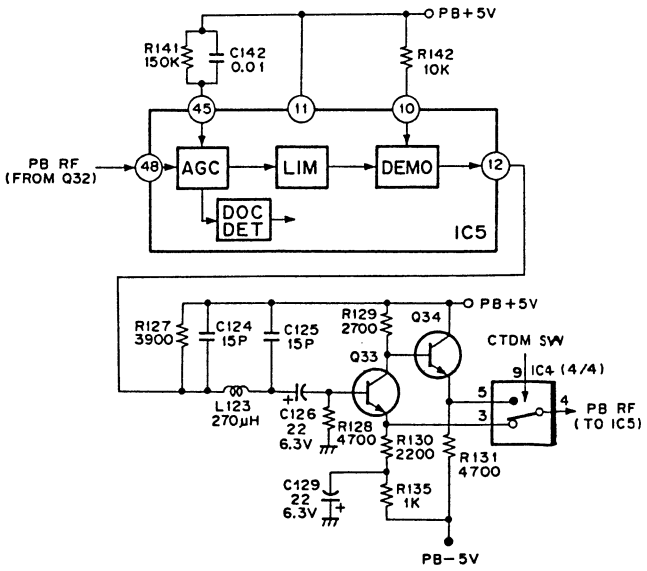



Fig. 2-20. FM Demodulator

R149 and C148 provide the de-emphasis time constants. The playback video signal (either Y RF or C RF signal) is amplitude adjusted by RV141 and feeds to pin 35 of IC5 output. This output signal is buffered by Q51, passed through C149 and sent to pin 37 of IC5 where the video signal takes two paths ; one path is the main line playback video signal while the other path is the playback video signal to be used for sync signal separation by feeding R152 and then pin 47 of IC5.

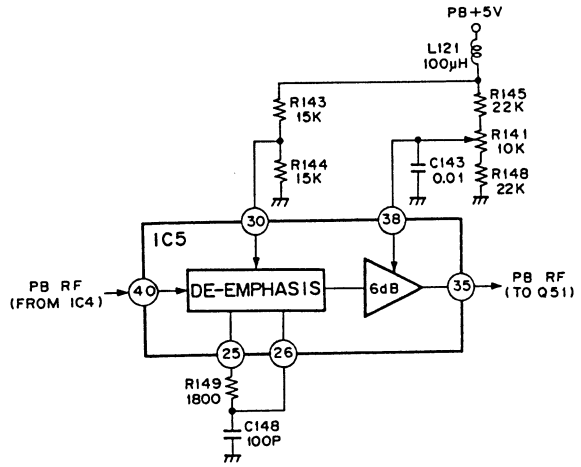



**Fig. 2-21. De-emphasis Block Diagram**

The playback video signal at pin 47 of IC5 is sent to the sync separator where the separated sync signal is obtained from pin 2 of IC5 and is returned to IC5 again through Q52. This signal clamps the main line playback video signal that is routed to pin 37 of IC5 input.

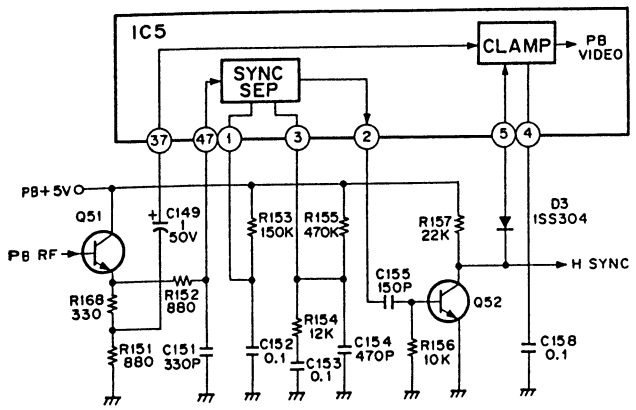



**Fig. 2-22. De-emphasis Circuit**

The clamped main line signal is passed through the reference sync muting circuit and buffer that are located inside IC5 and feed to pin 16 of IC5.
In order to arrange the playback video signal output from pin 16 of IC5 to Y signal with sync for the viewfinder, sync signal is waveform processed in the reference sync muting circuit. The reference sync muting circuit uses the Q52 output sync signal as its control signal. The equalizing pulse that is included in the sync signal is removed by IC7. The sync pulse width is determined by IC7, and is sent to pin 6 of IC7 where the horizontal sync tip of approximately 4.7 microseconds is added to the main line playback RF signal. The logic table of the control signal that is supplied to pin 6 of IC5 is shown as follows.

| IC5 PIN6 | INPUT LEVEL |
|---|---|
| OPEN | THROUGH |
| 0V | PEDESTAL |
| 5V | SYNC-TIP |

**Table 2-2.**

The back porch is added to the playback RF signal (either Y signal or CTDM signal) by Q54 and C160. The playback RF signal is sent from pin 16 of IC5 to viewfinder. Since the CTDM signal does not have vertical sync signal, the pseudo vertical sync signal of approximately 7H pulse width that is generated from switching pulse of the servo circuit, is added to the CTDM signal. The pseudo vertical sync signal is added to CTDM signal only during normal playback mode, and is added to the Y signal during FF/REW modes by Q58 so that the Y signal can have vertical lock on viewfinder even during the FF/REW mode (See Fig. 2-23.).

| MODE | SIGNAL | |
|---|---|---|
| | Y | CTDM |
| FWD | × | ○ |
| FF/REW | ○ | ○ |

○ : WITH PSEUDO V SYNC
× : WITHOUT PSEUDO V SYNC

**Table 2-3. Pseudo Vertical Sync Signal**

### 2-4-7. Dropout Compensator

The playback RF signal which is input to pin 48 of IC5, is passed through the AGC circuit and is sent to the dropout detector. Q55 is turned to ON by the dropout pulse that is supplied from pin 9 of IC5. By this circuit operation, the dropout period of the playback RF signal is replaced by the pedestal level by the reference sync muting circuit.

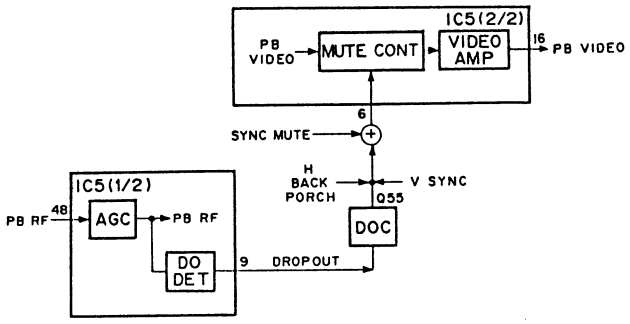



**Fig. 2-24. Dropout Compensator**

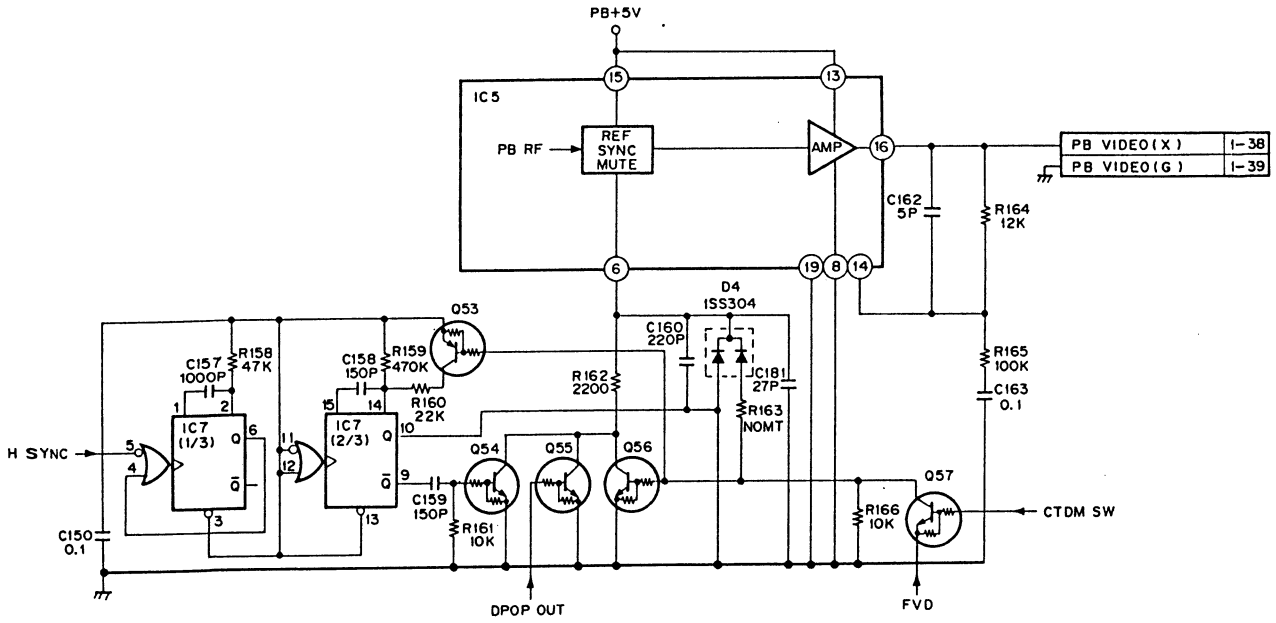



**Fig. 2-23.**

### 2-4-8. RF REC Pause Alarm Detector

When the machine is placed into the REC PAUSE mode, the tape turns a few fields due to back space edit, and one or two respective Y and C video tracks that have been recorded before the REC PAUSE mode are traced with all video heads. However, it is not sufficient for monitoring the recording condition of all video head directly, but to guess that the tape has been clogged or not by checking the all video heads with playback condition.

A sequence of detection is carried out by one field unit in order of Y1→Y2→Y3→Y4→C1→C2→C3→C4 and the machine will go into the ALARM state when missing any one playback signal is detected. As shown in Fig. 2-25, the playback RF signal output from each video head during PAUSE mode is triangle shape. This envelope is detected and sampled for 15th or 16th per field by the SY-117A board. When the RF is detected once during sampling, the unit does not go into the ALARM state.

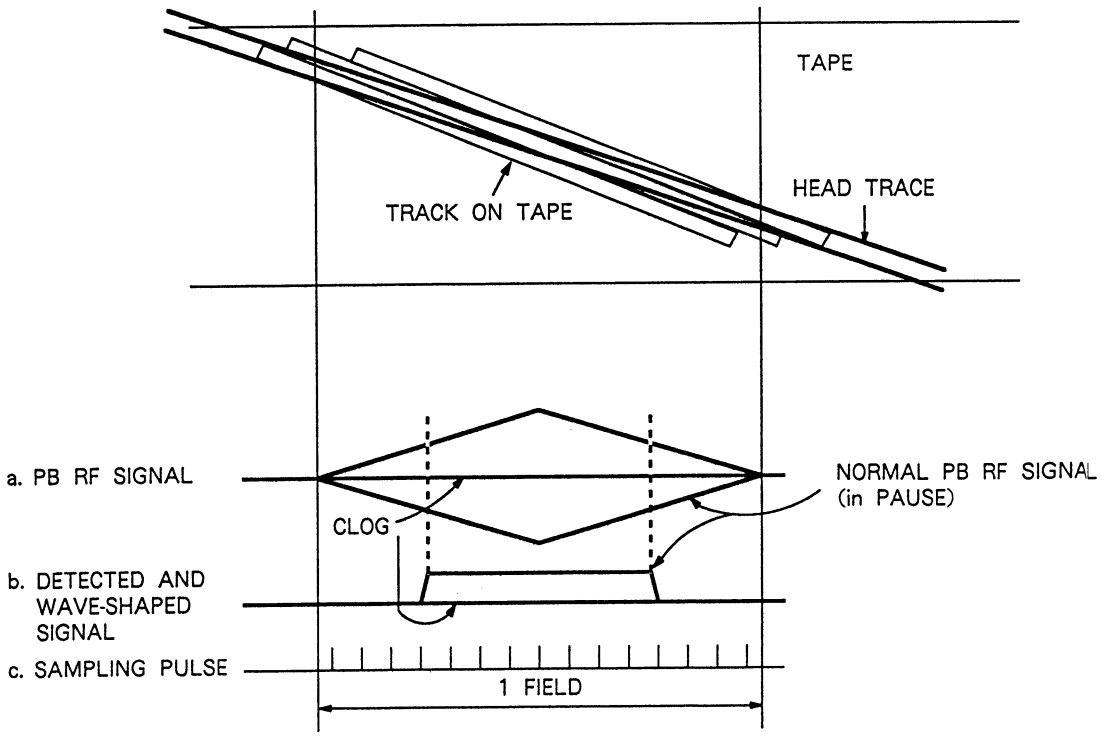



**Fig. 2-25. PB RF Signal in PAUSE Mode**

The Y and C PB RF signals are switched at IC4 by the control signal from the timing decoder IC3. After that, they are amplified and high frequency area are compensated for with Q36 and Q61. RV101 and RV102 are detection sensitivity adjustments. Both the METAL and OXIDE can compensate for with RV101 and METAL alone can compensate for with RV102. D1 is a detector. When decreasing the value of R110, detection sensitivity have increased because value of R110 have an effect on detection characteristics. A malfunction due to noise or dropout is reduced by the time constant R119 and C109.

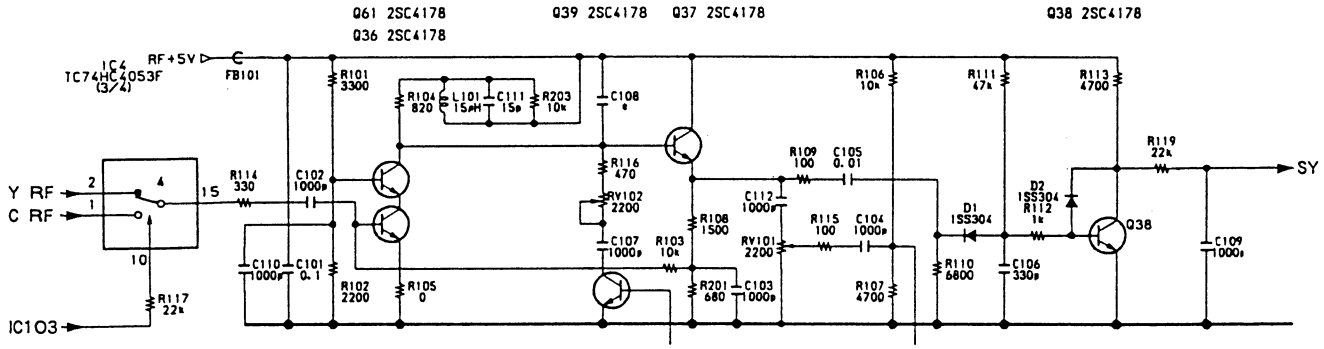



Fig. 2-26. RF Detector

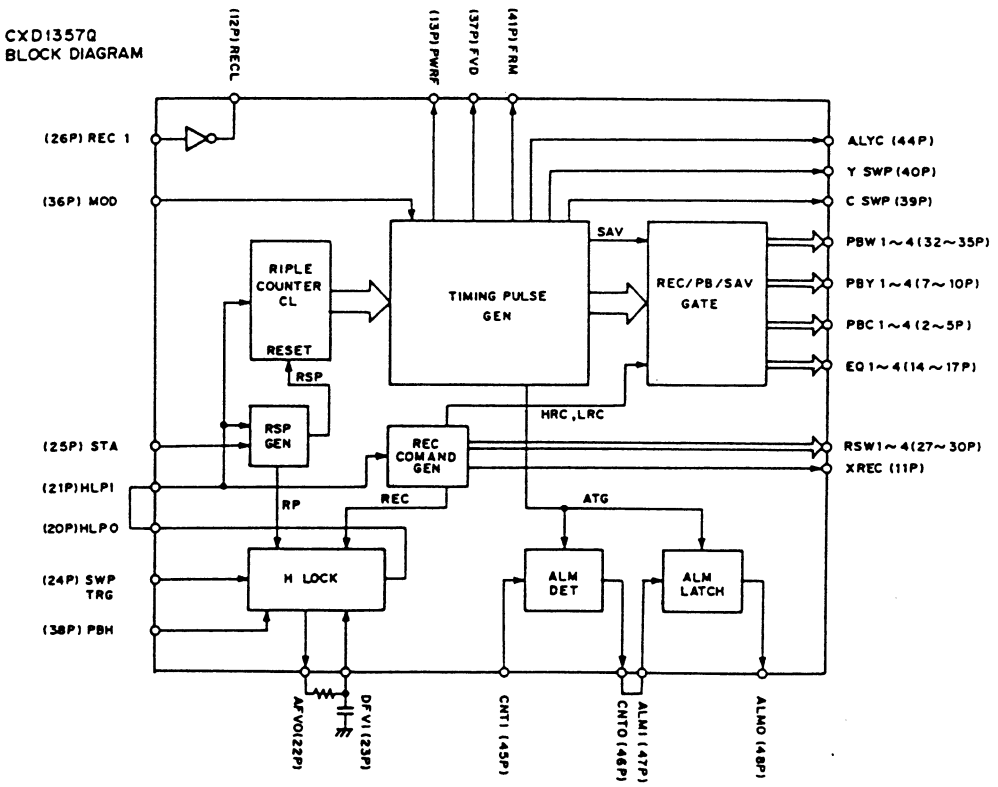



Fig. 2-27. Block Diagram

# SECTION 3
# AUDIO SIGNAL SYSTEM

## 3-1. OUTLINE

The audio signal system consists of the following boards.

- AFM-6 board
- AU-97 board
- TB-5 board
- FL-55 board
- TC-48A board
- VR-70 board
- MB-173A board
- PS-162 board

This equipment employs the Betacam SP format, so that recordings of both LNG audio 2 channels and AFM 2 channels are possible. The Dolby C noise reduction system is used for the LNG audio recording and can be turned on or off using a switch on the side panel of this equipment. When a METAL tape is used, the Dolby C noise reduction system is turned on automatically regardless of the DOLBY NR switch setting.

Three audio input connectors are provided: one input is exclusively prepared for microphone input (on the front panel) and the other two inputs are for MIC/LINE (on the rear panel). These input connectors are XLR-type, and each signals are supplied with balanced type connection. Power (+48 Vdc) of the phantom power supply is provided to all inputs connectors. These three input signals can select their recording channels by the audio input select switches (AUDIO IN). The audio signals that are recorded on the LNG audio CH-1 and CH-2, are recorded on the AFM CH-3 and AFM CH-4 at the same time respectively (Only when the metal tape used.) It is impossible to record the three inputs into separate channels.

This machine is mainly designed to use as recorder, the Dolby C noise reduction is not equipped. Also, the recording of the AFM signal is possible when the metal tape is used, but the playback function is not provided and the playback should be done by using the playback adaptor.

Audio signal levels are indicated by the liquid display panel in peak indication and audio channel 1 level can also be checked on the viewfinder.

## 3-2. RECORDING SYSTEM

Since the channel-1 and channel-2 have the same recording circuit configurations, description is provided only on channel-1.

### 3-2-1. Camera Microphone Amplifier

The standard input signal level for the microphone input is −60 dBu (0 dBu=0.775 Vrms). The input signal is sent to balanced amplifier IC151 on the MB-173A board. Q151 is a ripple filter for phantom microphone power supply. +48V is input to the microphone via resistors R161 through R169. The microphone signal is amplified by approximately 30 dB by IC151 and is sent to the TC-48A board.

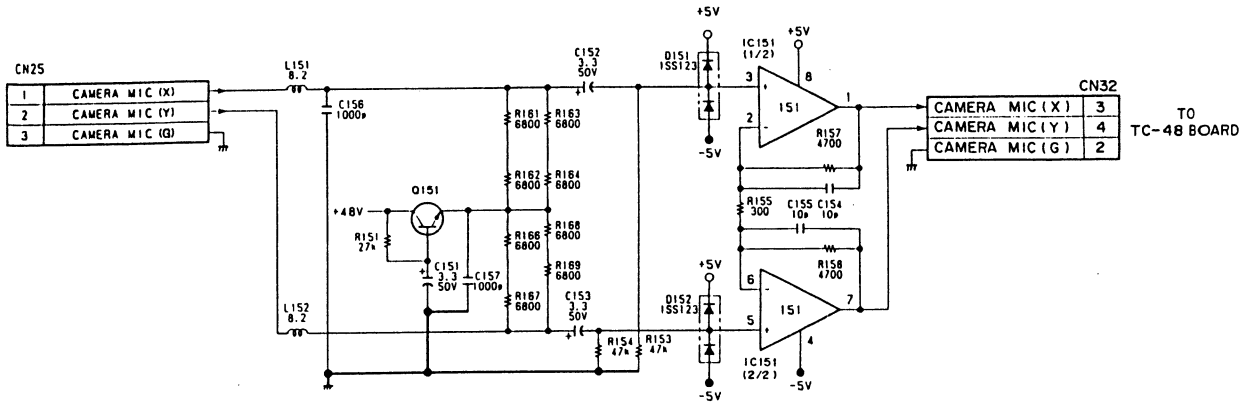



Fig. 3-1. Camera Microphone Amplifier

### 3-2-2. Microphone/Line Amplifiers

The signal input to the AUDIO IN CH-1 or CH-2 connector on the rear panel is sent to the IC101 on the TC-48A and either one of FRONT-MIC, REAR-MIC or REAR-LINE is selected using AUDIO IN switch (S101). When REAR MIC is selected by the AUDIO IN switch, the phantom power supply can be turned on or off using a switch located on the input connector for UC and EK models. The gain of IC101 is then set to 30 dB. When REAR LINE of the AUDIO IN switch is selected, the signal level is attenuated by approximately 33 dB by R101 through R108 and then sent to IC101.

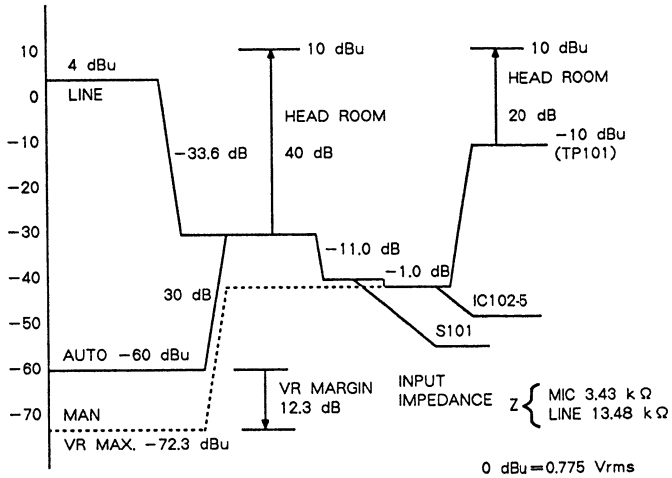



Fig. 3-3. Level Diagram

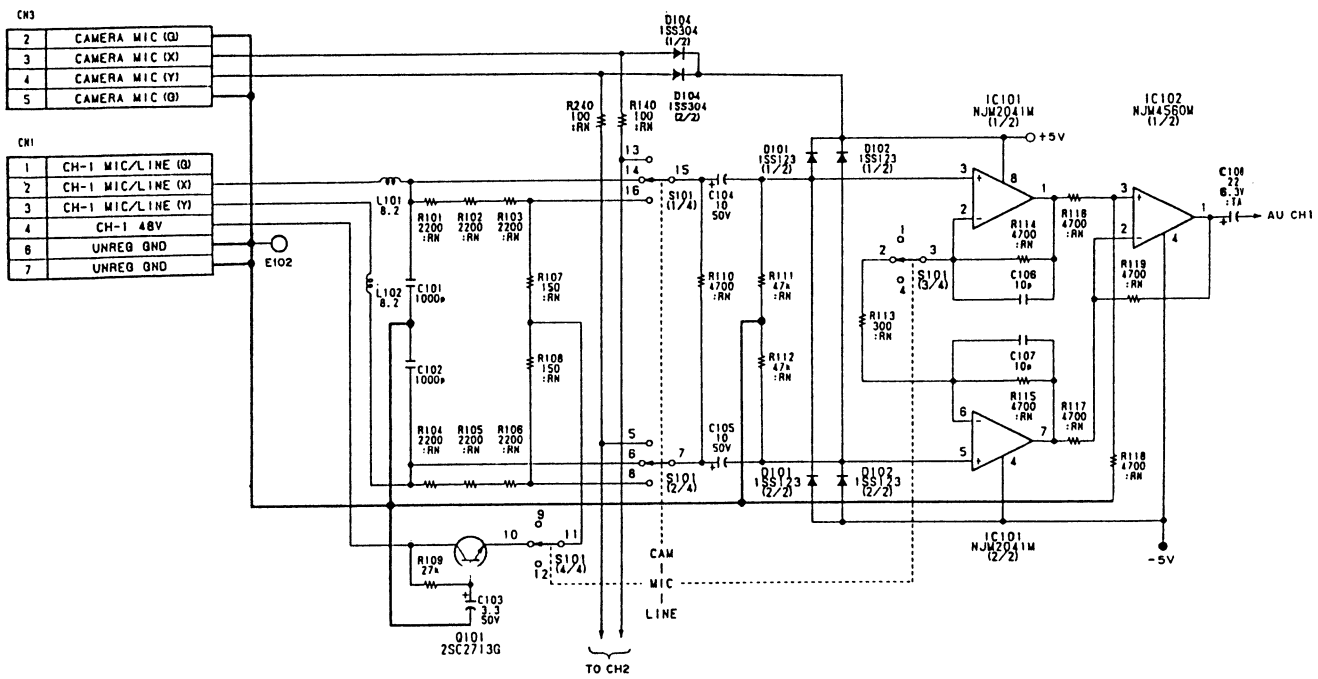



Fig. 3-2. Microphone/Line Amplifier

### 3-2-3. AGC and Limiter Circuits

The audio signal that is supplied from IC101 is input to IC102 (1/2) where signal is converted from balanced to unbalanced type. The signal which is converted to unbalanced using is level-controlled according to the mode selected by the AUDIO SELECT (AUTO/MAN) switch.

#### (1) AGC circuit

Audio signal during AUTO mode is attenuated to 11 dB by R120 and R121. It is then sent to IC102 (2/2) which is 32 dB amplifier. The IC102 output signal is sent to a full-wave rectifier consisting of IC103 and D103. The peak level of the full-wave rectified signal is detected using Q104, C111, C112, C113, R134 and R137. The resultant peak signal is sent to the gain controller Q102 via buffer Q107. The DC offset voltage (AGC reference level) for the full-wave rectifier circuit is produced by IC702 (1/2), IC703 and Q702. The offset voltage is obtained from the 3 Vdc that is output from pin 3 of IC703 and adjusted by RV701. When the signal level at TP101 is −10 dBu, the offset voltage is approximately 0.64V in normal temperature.

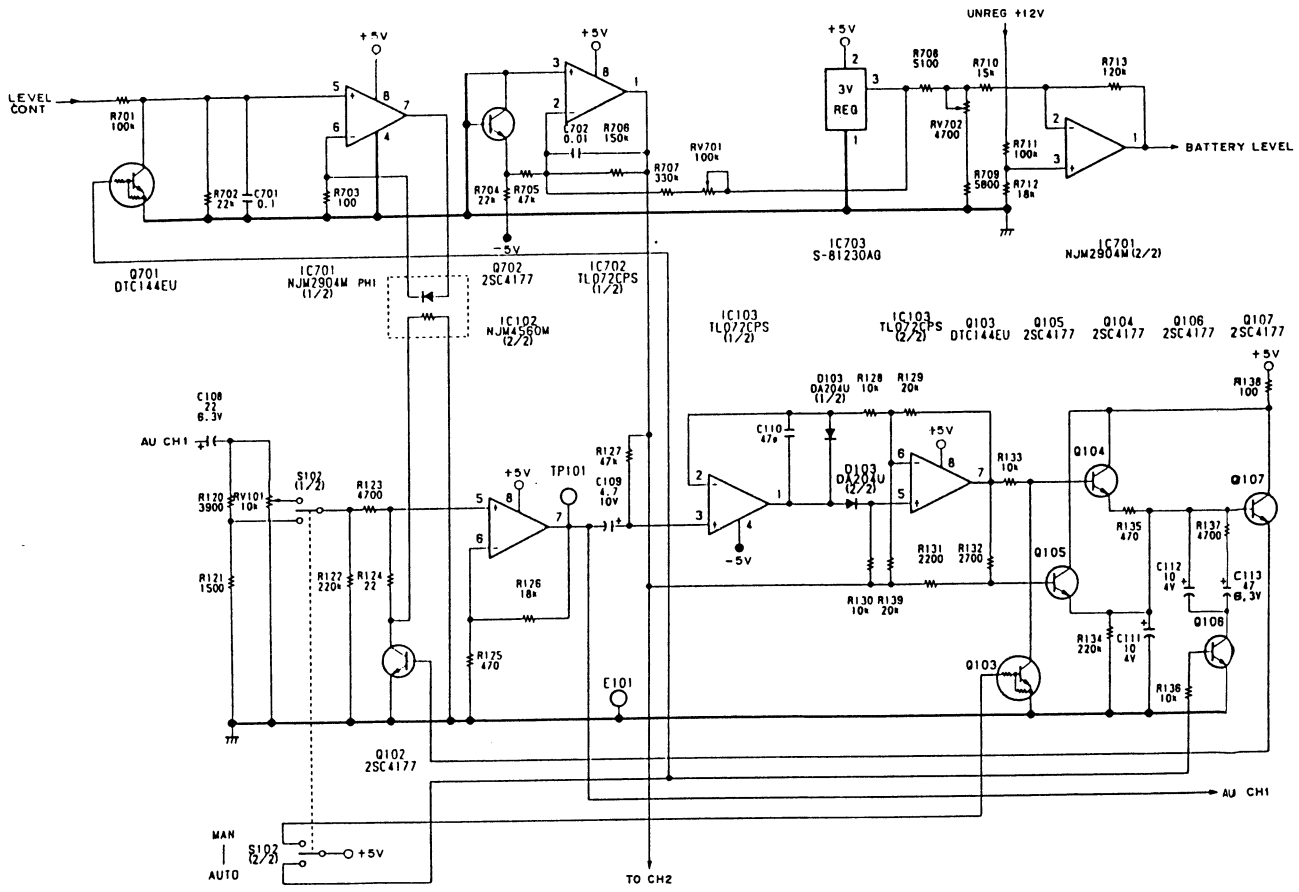



Fig. 3-4. AGC and Limiter Circuits

The Q702 is used as a temperature sensor to compensate for the temperature characteristics between the bases and emitters of Q102, Q104 and Q107.

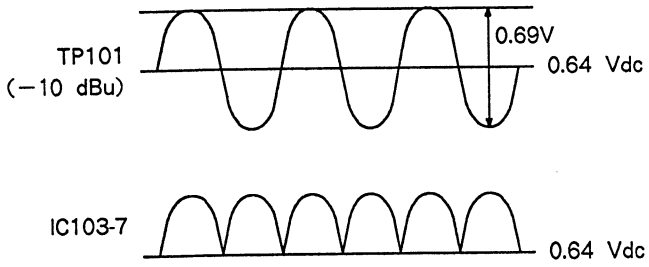



**Fig. 3-5. Full-wave Rectifier Waveform**

| INPUT (MIC) | OUTPUT (TP101) |
|---|---|
| −20 dBu | −6.2 dBu |
| −30 dBu | −6.8 dBu |
| −40 dBu | −7.4 dBu |
| −50 dBu | −8.2 dBu |
| −60 dBu | −10.0 dBu |

**Table 3-1. Input Level versus AGC Output Level**

In the AGC mode, the output audio signal from pin 7 of IC103 is sent to the base of Q104 via R133. When the AGC mode is established, Q106 is turned on so that the output from emitter of Q104 is sent to Q107 base via the integrator circuit of R135, R137, C111, C112, and C113. The impedance between the collector and emitter of Q102 can be changed by the Q107 emitter current by which the signal level is controlled.

**(2) Limiter circuit**

The limiter circuit is identical to the AGC circuit except that its operation point is 10dB higher than that of the AGC circuit by dividing the rectifier output voltage with R131 and R132. The time constant of an integrator circuit is also small in order to correspond to a more quickly rising-up signal. When the AUDIO SELECT switch is set to "MAN" mode, pin 7 of IC103 output is sent to the base of Q105. At that time, Q106 is off so that the time constant determined by R134, R143, C111 and C115 is connected to Q105 emitter.

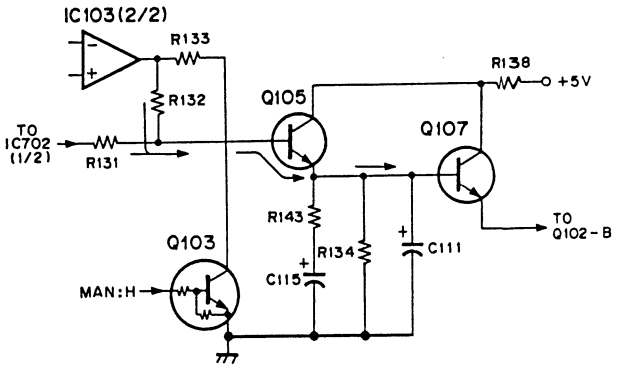



**Fig. 3-7. Limiter Circuit**

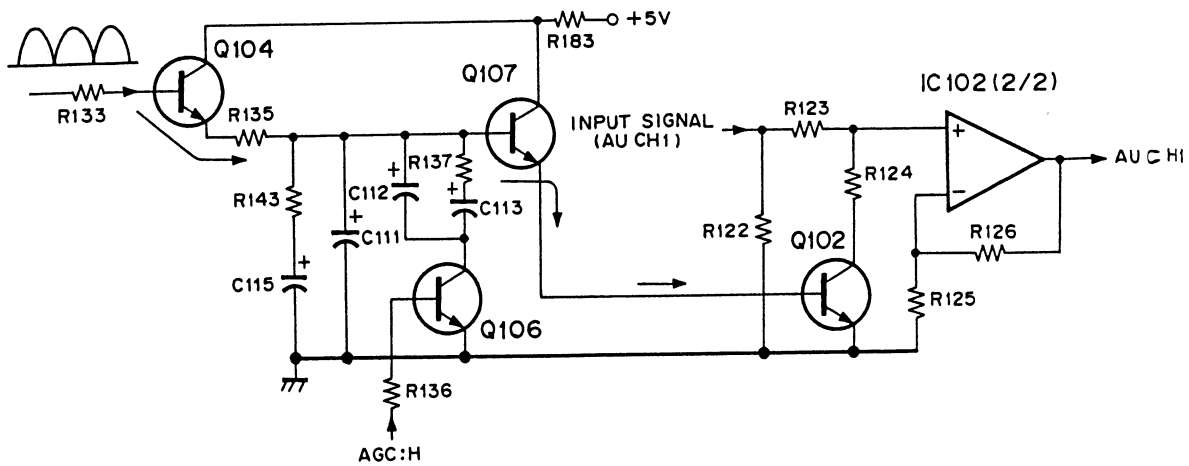



**Fig. 3-6. AGC Circuit**

### 3-2-4. CH-1 Input Level Controller

The input signal level of the AUDIO CH-1 can be adjusted by the photo-coupler PH1 connected in parallel between the base and collector of Q102 on the TC-48A board. Its internal resistance varies depending on the amount of light falling from LED. The AUDIO CH-1 input level can also be adjusted by the AUDIO LEVEL CH-1 control knob that is located in the viewfinder.

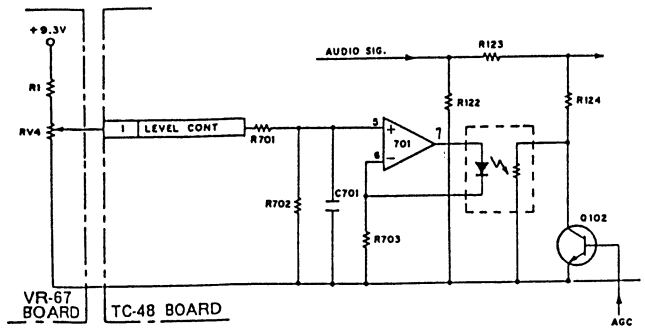



Fig. 3-8. CH-1 Input Level Controller

### 3-2-5. Dolby C Type NR System

The audio signal that is input to the AFM-6 board, is level-attenuated by 6 dB using R601, R603, R605, R607 and IC601 and the undesired frequency is eliminated by the low-pass filter (IC501). The resultant signal is sent to the AU-97 board. The IC102 on the AU-97 board is a Dolby C type NR encoder. The signal level at TP101 is adjusted to −10 dBu (when Dolby is off.) by RV101 when a reference signal is input.

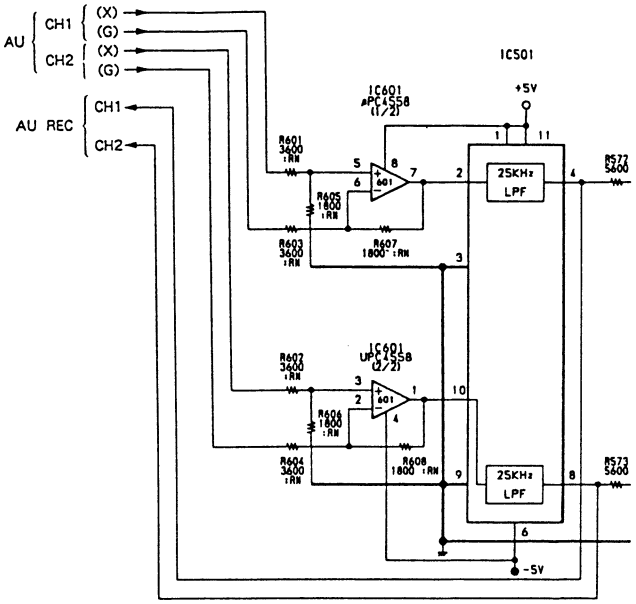



Fig. 3-9. LPF

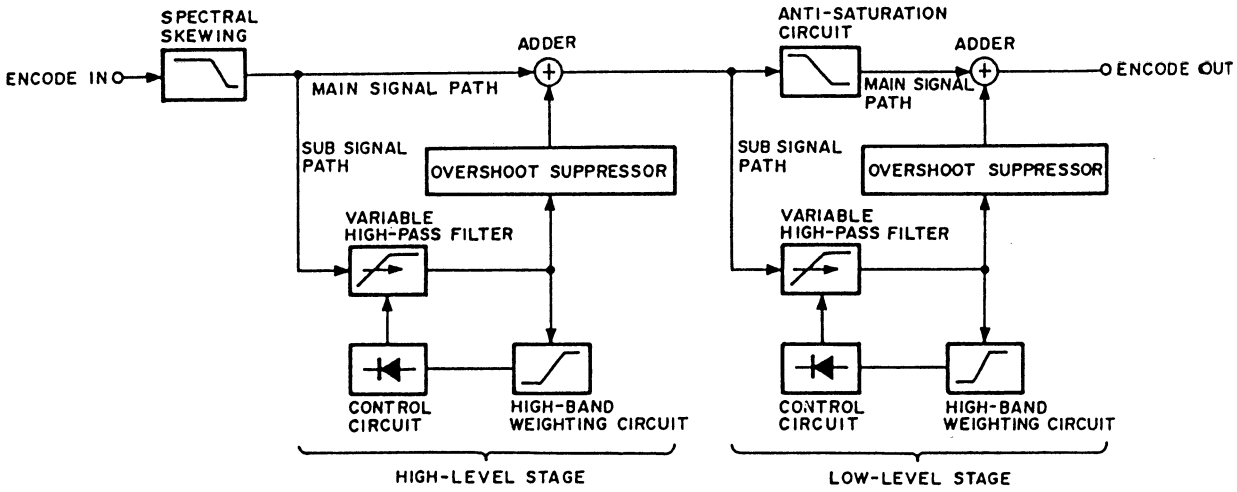



Fig. 3-10. Dolby C Type NR Circuit

### 3-2-6. Recording Equalizer

The IC111 (1/4) and IC111 (2/4) are the record equalizer for the oxide tape. The IC111 (3/4) and IC111 (4/4) are the record equalizer for the metal tape. These equalizers are equalizing the mid and high frequency ranges. The metal or oxide is selected by IC112 (1/2). The selected signal is then sent to the low frequency range equalizer IC131 (1/2) and peripheral circuit. A 134 kHz bias is added using CV131, and the resultant signal is sent to the record/playback selector on the FL-55 board. The record/playback selector consists of the relay (RY1) and Q1/Q11.

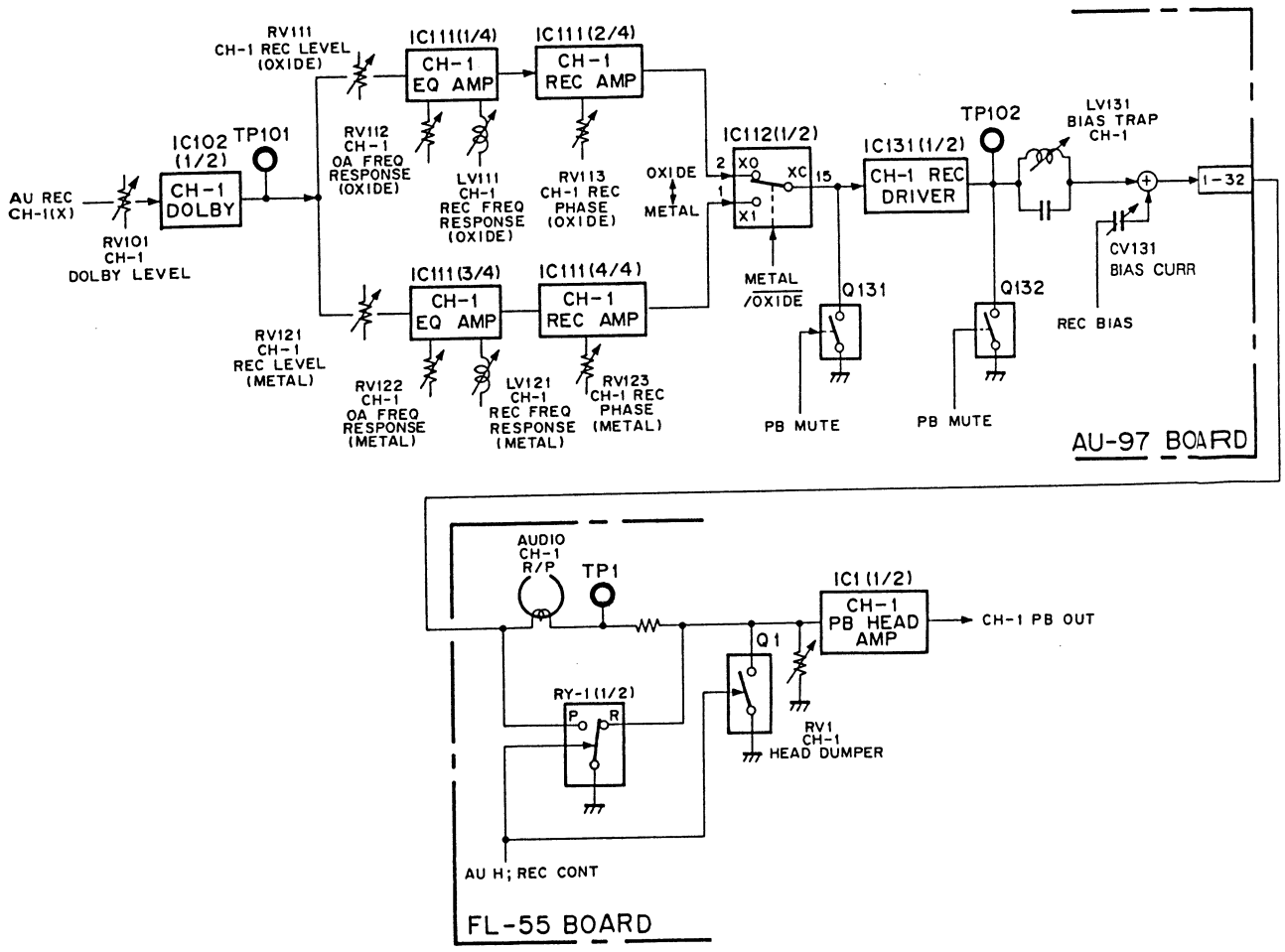
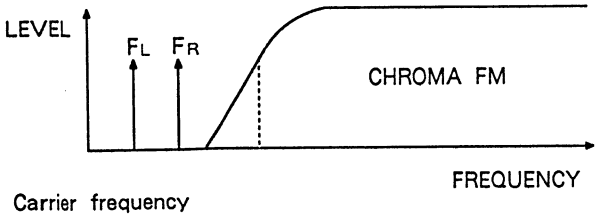



Fig. 3-11. Recording Equalizer

## 3-3. AFM SYSTEM

The AFM system is the audio recording system where an audio signal is frequency modulated and is frequency-multiplexed with the FM-modulated chroma signal for recording. In the Betacam SP format, the frequency spectrum is as shown below.




Carrier frequency
CH3 : 310 kHz
CH4 : 540 kHz
Frequency deviation
±75 kHz (max)
±25 kHz (with 400 Hz as reference level)

**Fig. 3-12. Frequency Spectrum of AFM System**

The AFM circuit uses a compound type noise reduction circuit which secures a dynamic range of 80 dB.
The audio signal which is sent from the TC-48A board to the AFM-6 board is attenuated by 6 dB with R601, R603, R605, R607 and IC601, passed through a 25 kHz low-pass filter (IC501). The low-pass filter output signal is sent to the compressor IC502 where the signal is compressed by 1/2-logarithmic compression. The output signal is FM-modulated by IC503. Pin 18 of IC503 has FM signal of approximately 200 mVp-p, that is multiplexed with the chroma signal by the AFM mixer on the VDA-11 board.

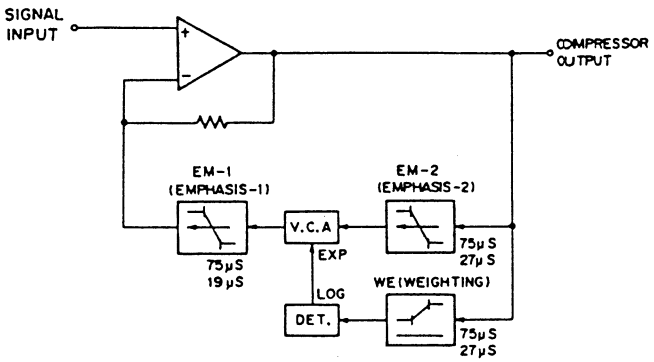



**Fig. 3-13. Compressor Basic Structure**

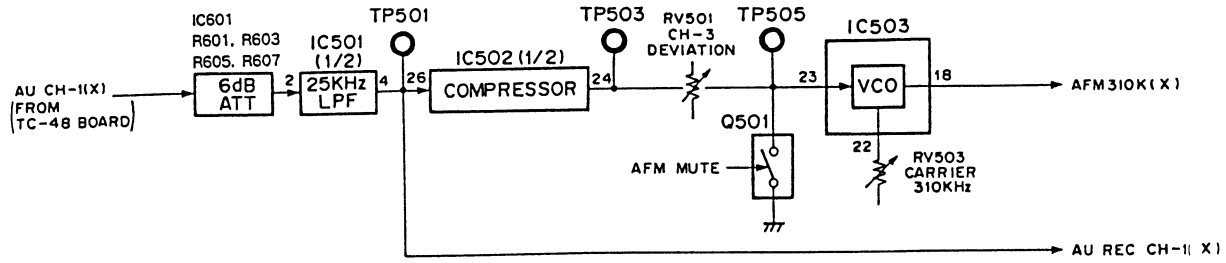



**Fig. 3-14. AFM System Block**

## 3-4. PEAK LEVEL METER CIRCUIT

The audio level is displayed on the LCD (Liquid Crystal Display) panel.
The IC301 on the TC-48A board is the PB/EE selector. The audio signal that is selected by IC301 is sent to a peak rectifier consisting of IC303 and D301. The peak-rectified signal is sent to the microprocessor IC503 and is analog-to-digital converted for LCD graphic display.

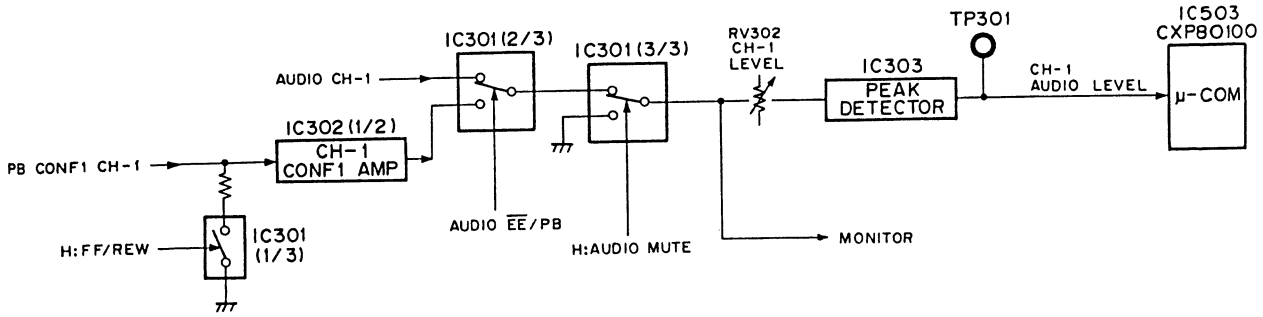



Fig. 3-15. Peak Level Meter Circuit

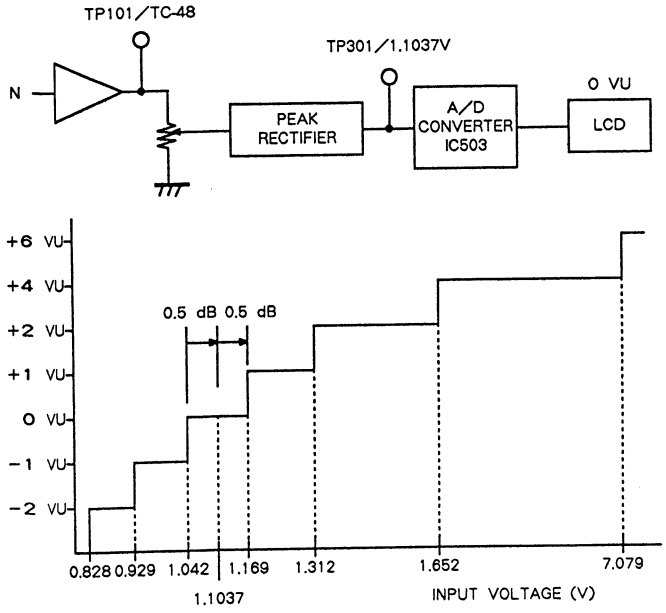
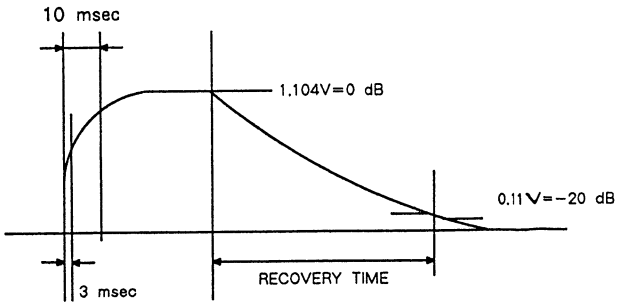



Fig. 3-16. Peak Level Meter Basic Structure




ATTACK CHARACTERISTIC

| | DIN STANDARD | BVW-200 |
|---|---|---|
| 3 msec | −4±1 dB | 4.4 dB |
| 10 msec | −1±0.5 dB | −0.8 dB |

RECOVERY CHARACTERISTIC

| | DIN STANDARD | BVW-200 |
|---|---|---|
| −20 dB | 1.5±0.2 sec | 1.56 sec |

Fig. 3-17. Chracteristics

## 3-5. BATTERY VOLTAGE DISPLAY CIRCUIT

The battery voltage is displayed in bar-graph on the LCD panel. A battery voltage of 10Vdc to 13 Vdc is converted into 0V to 3.51V and is analog-to-digital converted by the A/D converter inside the IC503 for LCD display.

When battery voltage reaches dc 11.30 Vdc, the "BATTERY" of the LCD panel blinks and the 1 kHz alarm sound will also be generated intermittently. The detecting voltage can be set in the range of 11.00 through 13.00 Vdc with 0.1V step.

When battery voltage reaches 11.00 Vdc, the "E" indication of the LCD panel will blink and the 1 kHz alarm sound will be generated continuously. When the battery end is detected, equipment operation is forced to stop and all modes except EJECT are disable.

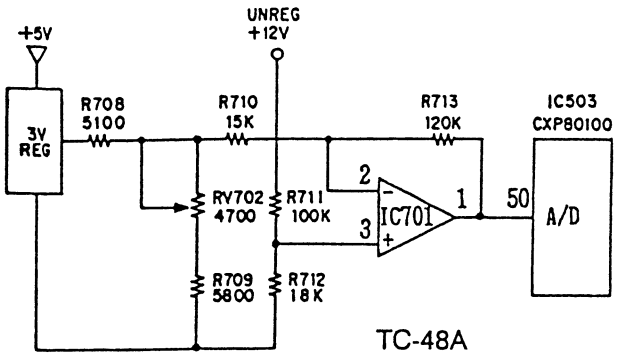



**Fig. 3-18. Battery Voltage Display Circuit**

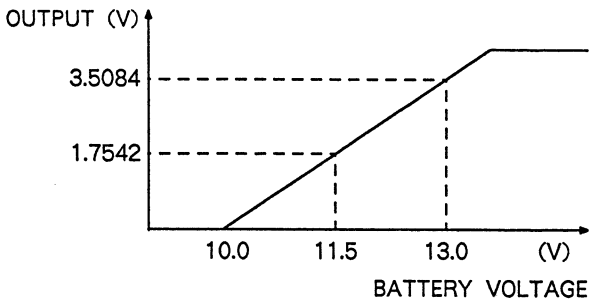



**Fig. 3-19. IC701 Conversion Characteristics**

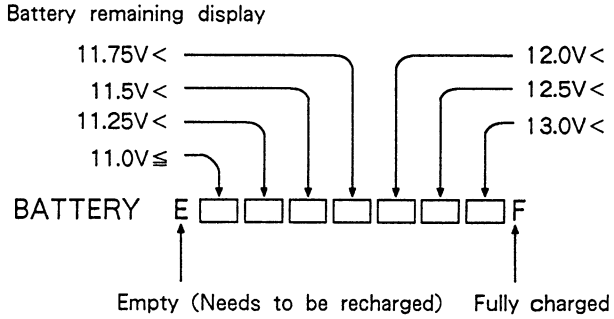



**Fig. 3-20. LCD Panel Display Content**

# SECTION 4
# SYSTEM CONTROL

## 4-1. OUTLINE

This equipment has one microprocessor that functions as the center of communication, in the system control block. This central microprocessor communicates with camera, audio, servo and time code blocks in the serial data communication format. Data transfer between the microprocessor in the system control with other boards are done as follows.

- System control → Camera : 2 bytes (Asynchronous)
- System control → Audio : 2 bytes (Synchronous)
- System control → Servo : 3 bytes (Synchronous)
- System control → Time code : 8 bytes (Synchronous)

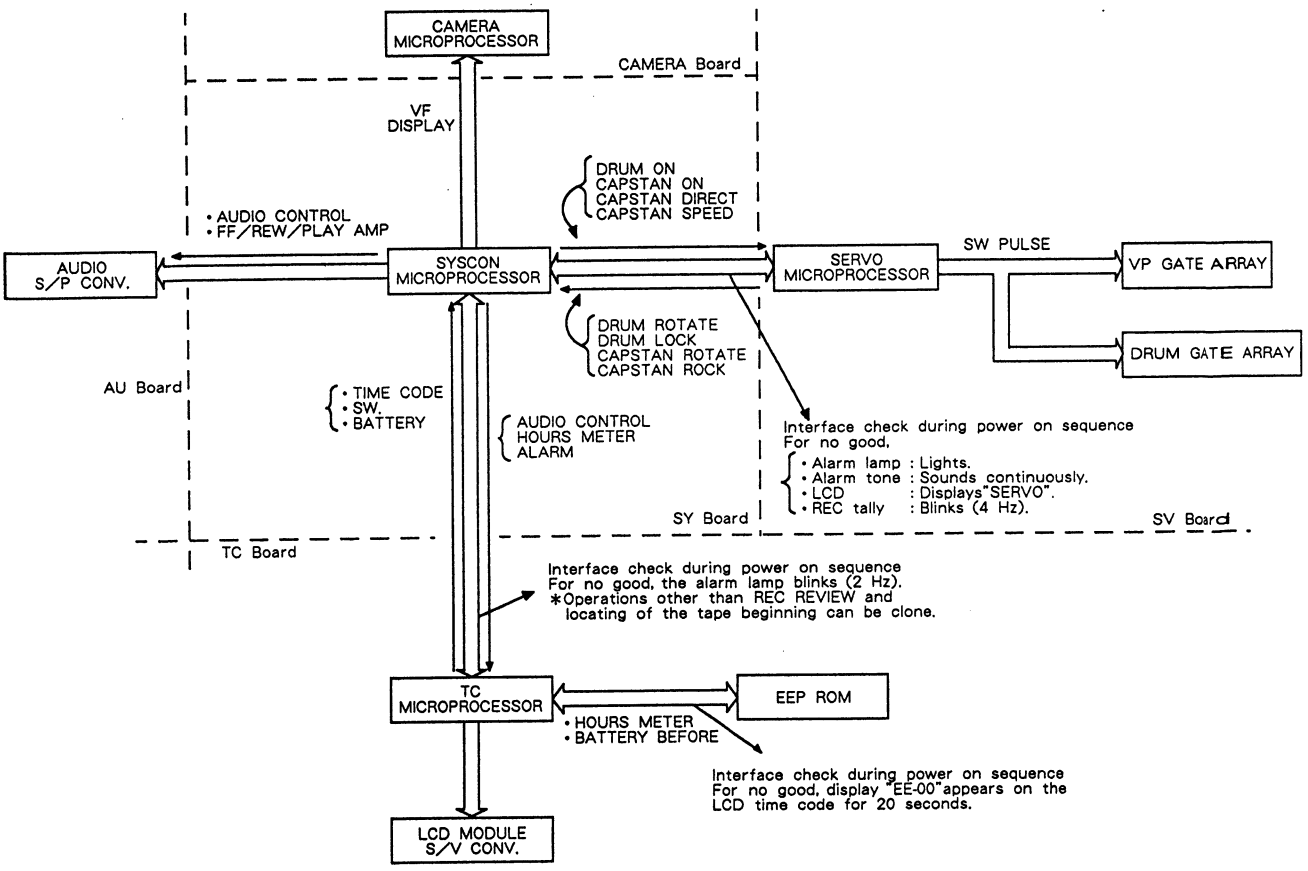



**Fig. 4-1. Outline of Interface**

## 4-2. SY-117A BOARD

The SY-117A board consists of microprocessor (IC1), reset circuit and output driver.

### 4-2-1. Microprocessor and Peripheral Circuits

The microprocessor and its peripheral circuits are composed as shown below.

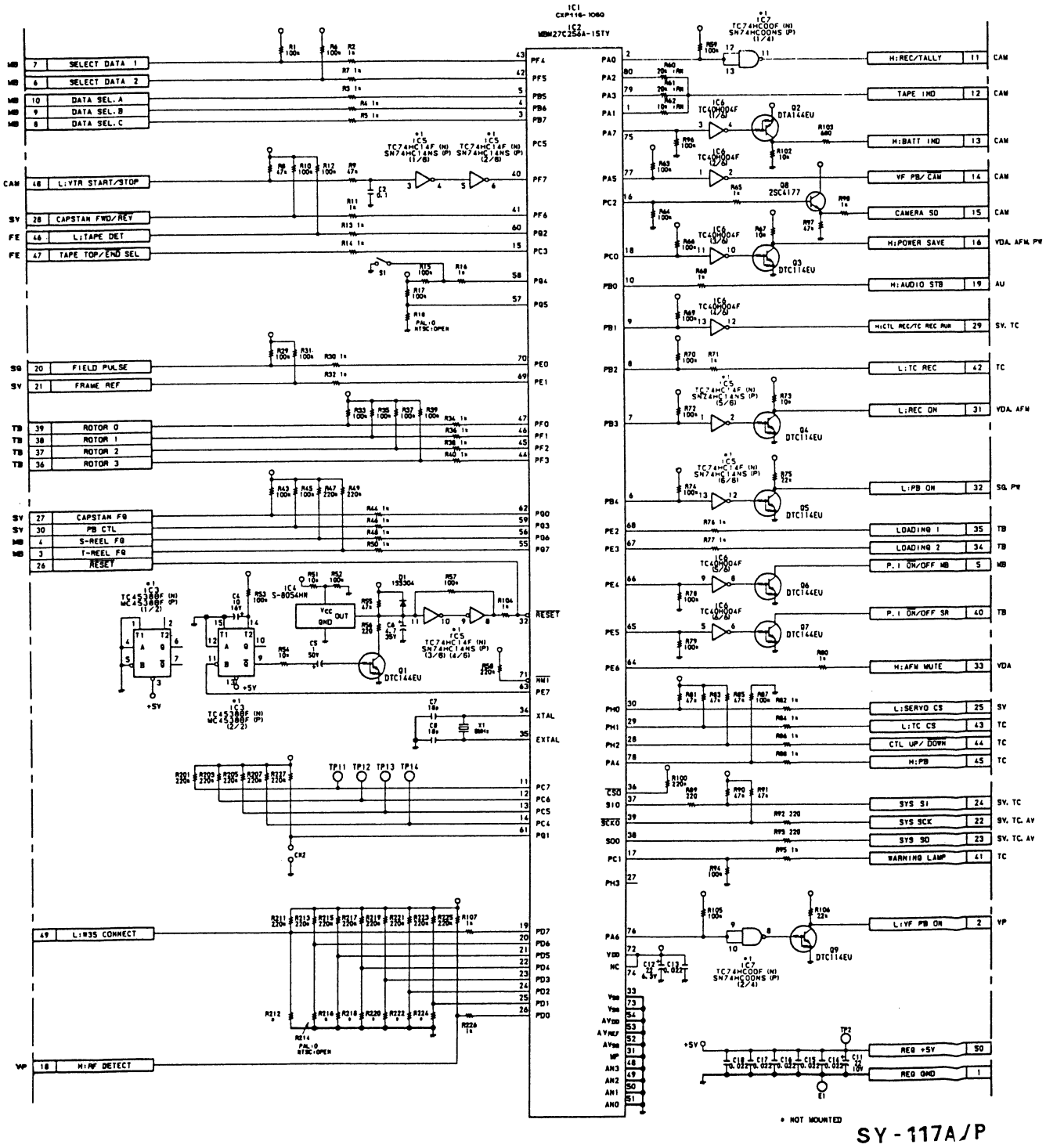



Fig. 4-2. Microprocessor and Peripheral Circuits

### 4-2-2. Microprocessor's Input/Output Signals

Input/output signals of the microprocessor (IC1) are described as follows.

**Pins 42/43 (PF5/PF4) :**
These are the input terminals for DATA 1 and DATA 2 signals that will be output from pin 14 of IC201 and IC202 on the mother board. Input data to be supplied through these pins are the key data, photo-coupler data and receiving READY data from other circuit blocks that are establishing the serial communication with microprocessor.

**Pins 3 to 5 (PB7 to PB5) :**
Data select output terminals of IC201 and IC202 on the mother board

**Pin 40 (PF7) :**
START/STOP signal input terminal depending upon the REC START switch condition of the VTR and camera

**Pin 41 (PF6) :**
Capstan rotation direction data input. Using this data, a selection signal is generated to determine that the tape sensor IC1 on the FE-4 board operates whether in REW direction or in FWD direction.

**Pin 60 (PG2) :**
Input terminal that receives the detection output of the TAPE TOP sensor and TAPE END sensor detectors

**Pin 15 (PC3) :**
Output terminal of the tape sensor select signal corresponding to pin 41 FWD or REW input signal

**Pin 58 (PG4) :**
Slack mute terminal. SLACK MUTE mode is established when this signal is set to Low. The SLACK MUTE is used when checking or adjusting the mechanism.

**Pin 57 (PG5) :**
PAL / NTSC select terminal. PAL mode is established when this terminal is Low. NTSC when High.

**Pin 70 (PE0) :**
Input terminal that accepts FIELD PULSE information from camera block

**Pin 69 (PE1) :**
Input terminal that accepts FRAME REF information from servo board

**Pins 44 to 47 (PF3 to PF0) :**
Input terminals that accept "function cam position" data input in the various operating modes

**Pin 62 (PG0) :**
CAPSTAN FG signal input terminal

**Pin 59 (PG3) :**
PB CTL signal input terminal

**Pin 56 (PG6) :**
S-REEL FG signal input terminal

**Pin 55 (PG7) :**
T-REEL FG signal input terminal

**Pin 32 (RESET) :**
Microprocessor reset pulse input terminal

**Pin 63 (PE7) :**
As long as CPU operates normally, the pulse of 2 msec rate is output from this terminal. When CPU should runs away, this terminal goes to High level that triggers the reset circuit of IC3, Q1 and IC5.

**Pins 34 and 35 (XTAL, EXTAL) :**
4 MHz crystal oscillator signal to be used for CPU clock should be connected here.

**Pins 11 to 14 and 61 (PC7 to PC4 and PG1) :**
Not used

**Pin 19 : (PD7)**
Not used (blank port)

**Pin 20 (PD6) :**
RF detection ON/OFF during recording

**Pin 21 to 25 (PD5 to PD1) :**
Not used (blank port)

**Pin 26 (PD0) :**
This terminal receives the RF detection signal input during REC PAUSE mode. This signal is used to determine ON/OFF of ALARM mode.

**Pin 76 (PA6) :**
Output for telling the VTR is in PB mode to the camera viewfinder

**Pin 17 (PC1) :**
WARNING lamp control signal output

**Pin 38 (SO0) :**
Serial data output

**Pin 39 (SCK0) :**
Output to supply the clock signal that is used for reading-out and writing-down the serial data.

**Pin 37 (SI0) :**
Serial data input

**Pin 78 (PA4) :**
Output of the signal to indicate that VTR is in PB mode.

**Pin 28 (PH2) :**
Output of the signal that determines up-count or down-count of the CTL pulse, depending upon the rotating direction of capstan.

**Pins 29 and 30 (PH1, PH0) :**
Output to send the enable signal to the CPUs on the SV-97 board and the TC-48A board at the timing to start communication when serial communication is attempted.

**Pin 64 (PE6) :**
AFM MUTE signal output

**Pin 65 (PE5) :**
Not used

**Pin 66 (PE4) :**
Output to turn off the photointerrupter in order to save power when initialization is completed, after the powre is turned on.
Output become on state when the VTR is set into the EJECT mode for waiting the cassette insertion, and when threading is completed, it is turned off after reading the photointerrupter information.

**Pin 67/68 (PE3/PE2) :**
Output to supply the control signals for the driving motor and driving block of the function cam mechanism.

**Pin 6 (PB4) :**
Output of PB ON signal.

**Pin 7 (PB3) :**
Output of REC ON signal.

**Pin 8 (PB2) :**
Output of TC REC signal.

**Pin 9 (PB1) :**
Output of CTL REC/TC REC RUN signal.

**Pin 10 (PB0) :**
Output of serial/parallel conversion control signal. When "High" level is output, serial/parallel conversion is performed. The serial/parallel conversion takes place after serial data is send out from pin 38, and the pin 10 is raised to this terminal goes "High" level.

**Pin 18 (PC0) :**
Output to send the power save signal to each boards during playback mode and EJECT mode when POWER SAVE is initiated.

**Pin 16 (PC2) :**
Output to send the self-diagnostic commands to the camera CPU. By this command, characters are displayed on the viewfinder.

**Pin 77 (PA5) :**
Output to send the playback mode/camera mode select signal. This signal is sent to camera viewfinder.

**Pin 75 (PA7) :**
Battery indicator signal output. This signal is sent to camera viewfinder.

**Pins 1, 79 and 80 (PA1, PA3 and PA2) :**
Output to send the tape remaining signal to the camera viewfinder. This data is A/D converted by the camera's CPU and is displayed on viewfinder.

**Pin 2 (PA0) :**
Output to send the REC TALLY lamp control signal.

### 4-2-3. Reset Circuit

The reset circuit consists of microprocessor IC1, IC3, IC4, IC5 and Q1. It has the following two functions :

**(1) Power ON reset circuit**

The power ON reset circuit consists of IC4, IC5 (3/6) and IC5 (4/6). The power ON reset circuit detects the power supply voltage (Vcc) to IC4 and sends the reset pulse to 32 pin of microprocessor. At the same time, reset signal is sent to the other microprocessor.

**(2) Resetting the watch-dog timer (when microprocessor should runs away)**

Microprocessor is detected whether it is normally operating or should runs away, by monitoring the output pulse of the pin 63 of the microprocessor with IC3 (2/2). As long as the microprocessor is operating normally, "Low" level is output from pin 9 of IC3. When the microprocessor should run away, Q1 is turned on and the microprocessor is reset.

# SECTION 5
# SERVO SYSTEM

## 5-1. OUTLINE

All the functions of the drum servo system and capstan servo system of this equipment are controlled by the CPU (IC1) on the SV-97 board.

## 5-2. SERVO CPU

The servo CPU (IC1 : CXP80116) is the high speed (500 nsec)/highly integrated CMOS type, single chip, eight-bit servo microprocessor. In order to make easy the control of VTR mechanism and servo control, the peripheral functions are also built inside the CPU. The CPU includes the following functions too.

- ROM (16 Kbytes)
- RAM (352 bytes)
- A/D converter (8-bit/8-channel, sequential comparison system, conversion time : 20 $\mu$ sec)
- Serial I/O (1 to 8 bytes automatic transfer, built-in 8-stage FIFO for data)
- I/O port
- Timer counter
- Time base timer
- Vector interrupt
- High speed timing pattern generator
- PWM generator
- PWM/DA gate pulse output circuit (12-bit/2-channel)
- Vertical sync separator
- Capstan FG circuit (with built-in divider)
- Drum FG/PG circuit
- CTL circuit (with built-in divider)
- Free-running counter (built-in 6-stage FIFO for FRC data)
- Power on reset function
- Sleep/stop function
- External memory expansion mode

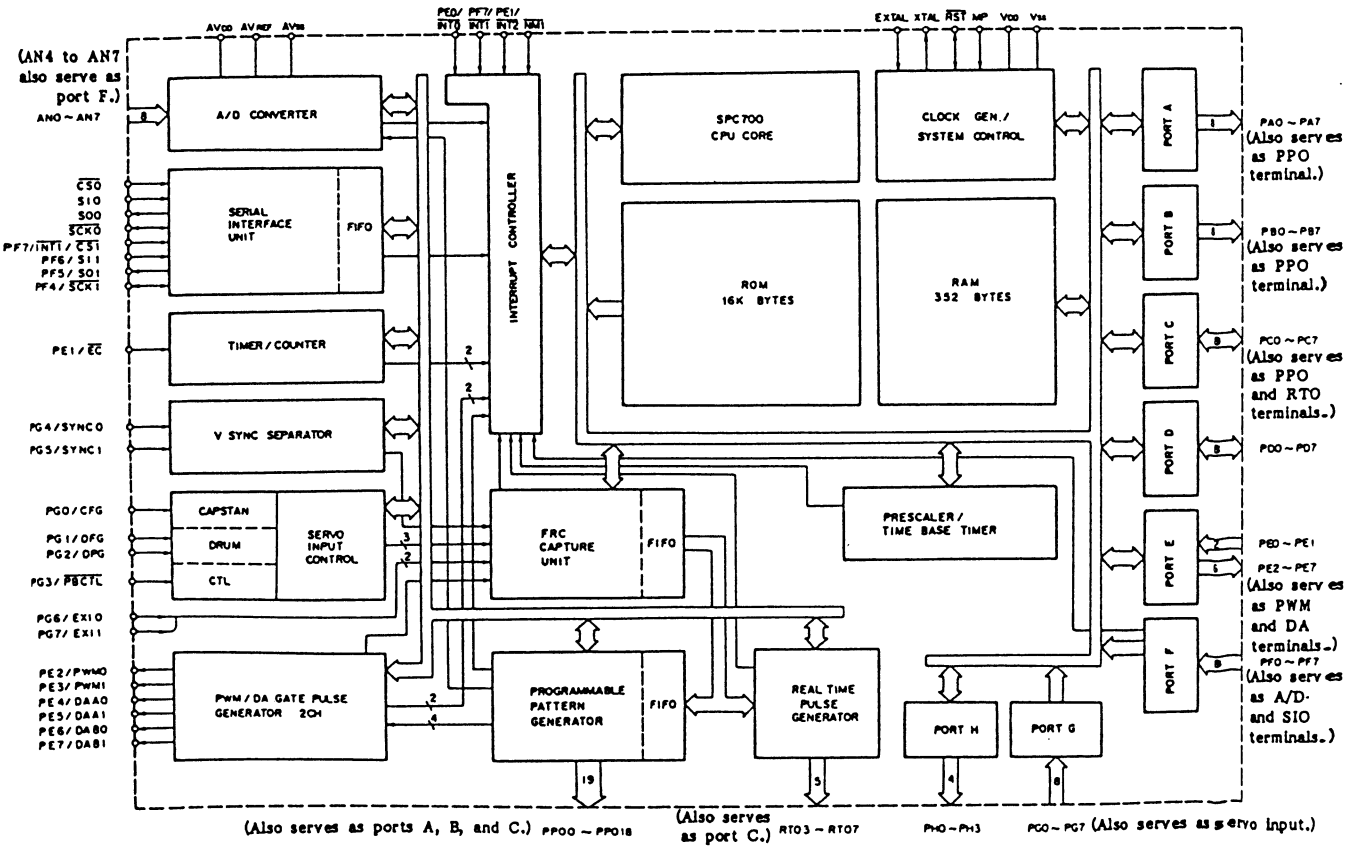

(AN4 to AN7 also serve as port F.)
AN0 ~ AN7
A/D CONVERTER
SERIAL INTERFACE UNIT
FIFO
TIMER/COUNTER
V SYNC SEPARATOR
CAPSTAN
DRUM
CTL
SERVO INPUT CONTROL
PWM/DA GATE PULSE GENERATOR 2CH
INTERRUPT CONTROLLER
SPC700 CPU CORE
CLOCK GEN./ SYSTEM CONTROL
ROM 16K BYTES
RAM 352 BYTES
FRC CAPTURE UNIT
PRESCALER/ TIME BASE TIMER
PROGRAMMABLE PATTERN GENERATOR
REAL TIME PULSE GENERATOR
PORT A
PORT B
PORT C
PORT D
PORT E
PORT F
PORT H
PORT G
PA0 ~ PA7 (Also serves as PPO terminal.)
PB0 ~ PB7 (Also serves as PPO terminal.)
PC0 ~ PC7 (Also serves as PPO and RTO terminals.)
PD0 ~ PD7
PE0 ~ PE1
PE2 ~ PE7 (Also serves as PWM and DA terminals.)
PF0 ~ PF7 (Also serves as A/D and SIO terminals.)
(Also serves as ports A, B, and C.) PP00 ~ PP018
(Also serves as port C.) RT03 ~ RT07
PH0 ~ PH3
PG0 ~ PG7 (Also serves as servo input.)

Fig. 5-1. Internal Structure of CPU

The free running counter (FRC) that is located inside the CPU, has 19-bit structure. It receives the PS0 (125 nsec, fex : 8 MHz) from pre-scaler as the clock signal. Content of this FRC counter can be cleared by pulling the RST terminal to "Low" level, but it cannot be cleared by means of software control.

The FRC is for measurement of input signal inside the FRC capture unit, and is used as the reference clock for peripheral hardware. The FRC counted output values are sent to the PPG (Programmable Pattern Generator) and to the RTG.

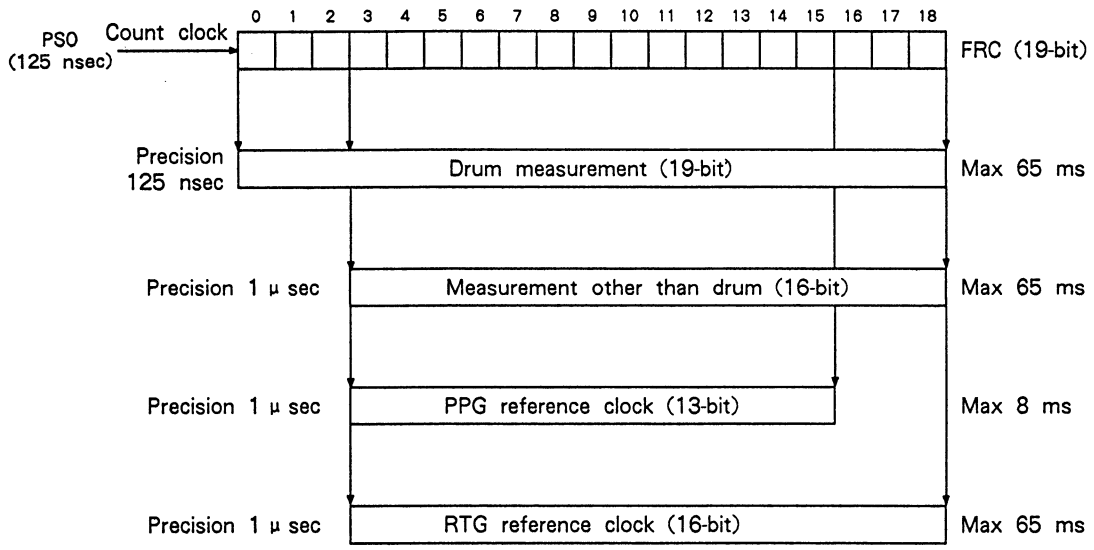

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
PS0 Count clock
(125 nsec)
FRC (19-bit)
Precision
125 nsec
Drum measurement (19-bit)
Max 65 ms
Precision 1 μ sec
Measurement other than drum (16-bit)
Max 65 ms
Precision 1 μ sec
PPG reference clock (13-bit)
Max 8 ms
Precision 1 μ sec
RTG reference clock (16-bit)
Max 65 ms

**Fig. 5-2. Structure of Free-Running Counter (FRC)**

## 5-3. DRUM PG WAVEFORM SHAPER

The drum PG pulse is produced one output pulse per every rotation of head drum motor. Since this equipment employs the special small size head drum, rotating speed of head drum 1.5 times of conventional models. This means that the phase servo of head drum is controlled by 37.5 Hz signals. The drum PG pulse output is wave-shaped by Q1 and is sent to monostable multivibrator IC12 (2/2) where pulse width become constant and then sent to the servo CPU.

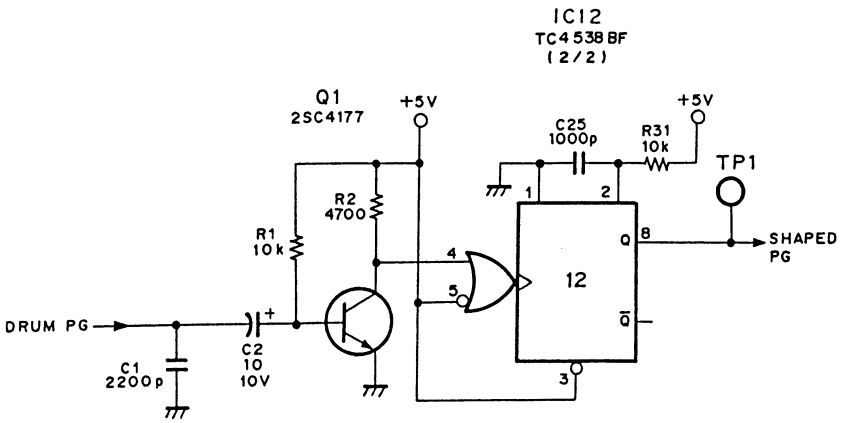



**Fig. 5-3. Drum PG Waveform Shaper**

## 5-4. DRUM/CAPSTAN FG WAVEFORM SHAPER

The drum FG waveform shaper and the capstan FG waveform shaper have the same circuit configuration. The input FG signal is amplified by IC2, converted into a rectangular waveform by comparator IC3 and is sent to the servo CPU. Servo CPU measure the rise-up time of the FG signal, by which the drum rotating speed and capstan rotating speed are measured. The measured error data are D/A converted and are sent to outputs.

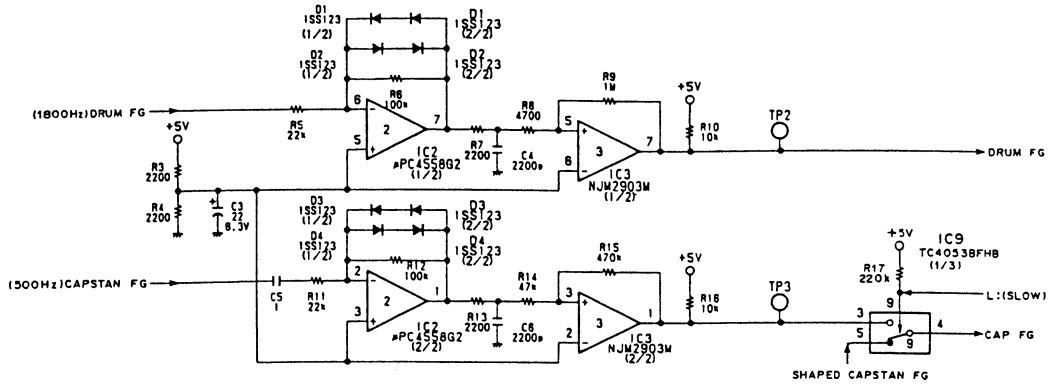



Fig. 5-4. Drum/Capstan FG Waveform Shaper

## 5-5. MOTOR DRIVE PWM AMPLIFIER

The head drum motor driver and the capstan motor driver have the same circuit configuration. The head drum motor driver alone is described as follows.
The input head drum error voltage is D/A converted by the servo CPU and IC16 (2/2) and is sent to the PWM amplifier consisting of IC18 (2/2), IC17 (1/2), IC19 (1/2) and Q3. The error voltage is amplified and phase-compensated by the IC18 (2/2) and is sent to the comparator IC17. The IC19 (1/2) is the sawtooth wave generator that will be used for sampling in the PWM. The PWM clock frequency is selected about 44 kHz in order to prevent beat with the AFM carrier signal or to cause deterioration of SN ratio of the longitudinal audio signal. The sawtooth wave signal from IC19 (1/2) is compared with the drum error voltage at IC17 (1/2) and modulated to a PWM. Therefore ON/OFF duty of Q3 is controlled.
This circuit has the negative feedback in order to stabilize the loop gain and to prevent from the adverse effect from the fluctuations of the power supply voltage. In addition, Q4 and Q5 are the circuit for braking the motor.

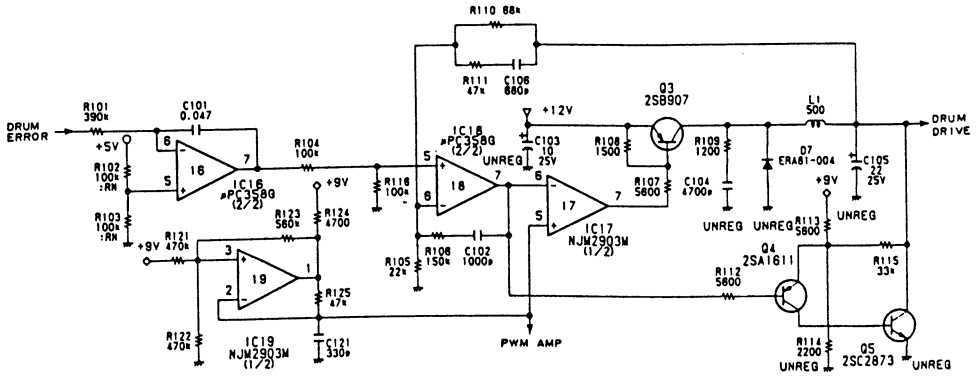



Fig. 5-5. Motor Drive PWM Amplifier

## 5-6. CAPSTAN STOP SERVO

The capstan servo uses the capstan FG (A) signal and the capstan FG (B) signal that are 90° out of phase each other and are generated together with the rotation of the capstan motor rotation. These FG signals are generated by the FG ring and DMEs (Divided Magneto Element) attached inside the capstan motor. When the capstan motor is rotating in the FWD direction, the 90° phase advancing signal is called as FG (A). Other signal is called FG (B). The FG (A) signal that is input to pin 35 of CN11 (50-pin) is amplified by IC4 (1/2) where signal is amplified and phase compensated, is full-wave rectified by IC6 to become the stop error signal. This stop error signal replaces the capstan servo error signal and is sent to the capstan motor as the capstan drive voltage through the PWM amplifier. The stop servo has the following functions as well :

- Rotating speed detection
  (Selection of capstan error and stop error)
- Rotating direction selection
  (Capstan rotationg direction control)
- Rotating direction detection
  (Control of rotating direction selection)

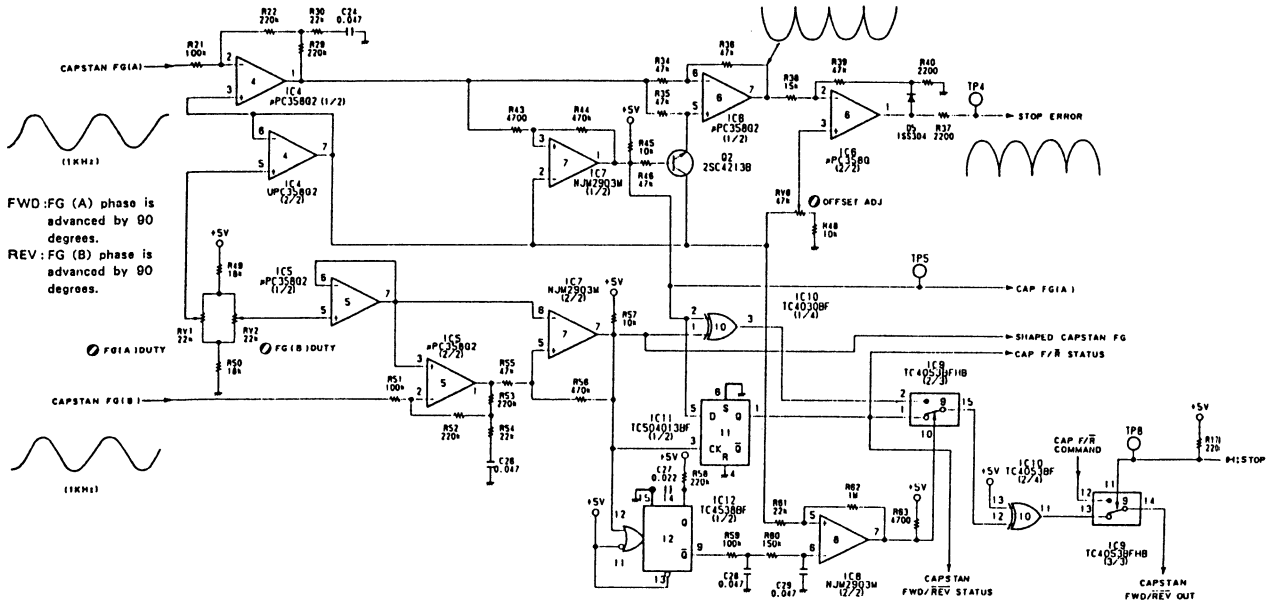



Fig. 5-6. Capstan Stop Servo Circuit

### 5-6-1. Rotating Direction Detection

The rotating direction of the capstan motor is detected by using the phase difference between FG (A) and FG (B) after then are shaped into rectangular pulse by IC7. Detection of rotating direction is carried out by IC11 (1/2). This data is sent to the servo CPU and system control CPU where it is employed for controlling the selection of capstan motor rotating direction when in STOP.

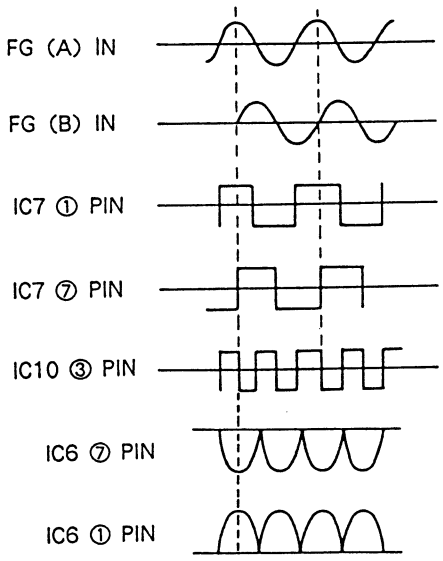



Fig. 5-7. FG (A) and FG (B)

### 5-6-2. Rotating Speed Detection

If the capstan rotating speed is too fast (about 1/6 times the normal or more), it cannot be stopped by the stop servo alone. In this case, a reverse command is sent once to the capstan motor and is then replaced by the stop servo mode command after the rotating speed becomes slow enough (about 1/6 times the normal). So, the capstan stop servo circuit is equipped with the simple speed detector circuit. In this circuit, the wave-shaped FG (B) signal is sent to the monostable multivibrator IC12 (1/2) to generate the pulse. The output pulse is integrated and the integrated output value is compared with the reference voltage by the comparator IC8 for the capstan speed detection. IC8 outputs "High" when the rotating speed is fast and "Low" when the rotating speed is slow.

### 5-6-3. Rotating Direction Change

Purpose of "rotating direction change" circuit to stop the capstan motor at the specified position and to maintain this state. The rotating direction of the capstan is controlled by the stop error command by using the rectangular-wave-shaped FG (A) and FG (B) signals.
The capstan motor is stopped at the position shown by Fig. 5-8① (dip point of stop error). When the capstan motor is about to rotate from this point, the signal to let the motor rotate in opposite direction (Fig. 5-8②) is generated so that the capstan motor is kept stand still.

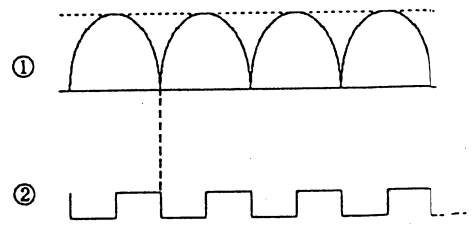



Fig. 5-8. Rotating Direction Change Waveform

## 5-7. BACK-SPACE EDITING

When the VTR's START/STOP switch is pressed during record mode, the VTR enters the back-space edit mode where the tape is rewound by 7.5 CTL equivalent length and stopped. During this tape rewinding, the number of capstan FG is counted from the record end point for tape length measurement. When the VTR's start/stop switch is pressed again, the capstan start command is sent from the system control to the servo CPU. In order to in-phase the 1/2VD and PB CTL at the recording point, the servo CPU generates the compensation for the time delay until the actual start of the capstan motor, and starts the motor in synchronizing with 1/2VD. This delay time can be adjusted by RV5 on the SV-97 board. As the capstan motor starts up and reaches near the specified rotating speed, phase of PB CTL signal and 1/2 VD signal are in phase by the phase servo. The CTL record command given from system control to CPU so that the continuity of CTL signal is maintained even at the back-space edit point.

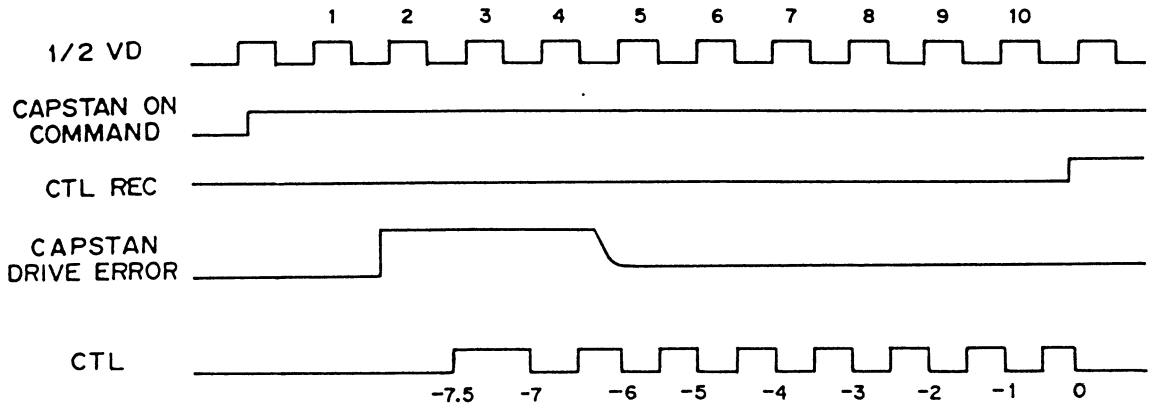



**Fig. 5-9. Back-Space Editing**

## 5-8. SYNC DETECTOR

The composite sync supplied from camera block to pin 58 (SYNC 0) of servo CPU (IC1) is used as reference signal of the servo system. However, when make a playback with connecting the TBC to playback adaptor, it is necessary to meet the lock phase of playback servo to TBC. When the advanced (ADV) sync signal is supplied from the TBC to the SV-97 board through the playback adaptor, ADV sync is detected by Q9 and Q10 and the ADV sync signal is selected as the servo reference signal.

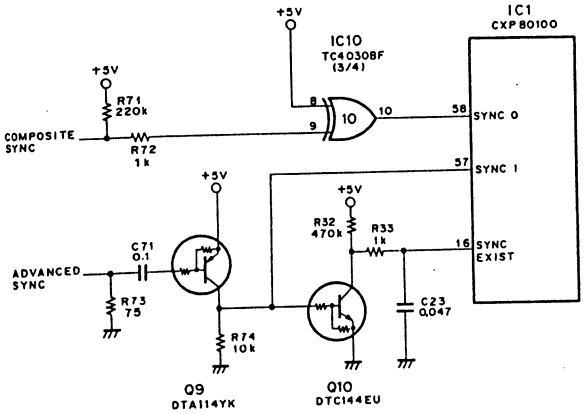



Fig. 5-10. Sync Detector

## 5-9. CTL RECORD/PLAYBACK AMPLIFIER

In the Betacam format, the 1/2 VD signal after it is delayed by 1.5H is used as the CTL signal recorded on the tape. Recording of the CTL signal is performed by IC22 and IC14 (1/3). IC22 controls record ON/OFF of this signal and IC14 (1/3) reverse the polarity of the record current flowing in the head. The signal output from the CTL head during playback mode is sent to the circuit consisting of IC121 and IC122 on the MB-173A board and amplified, and is then sent to the SV-97 board. This PB CTL signal input to the servo board is wave-shaped by IC15 (1/2) and sent to the servo microprocessor. The servo CPU controls so that the phases of the wave-shaped PB CTL and 1/2 VD signal are in phase.

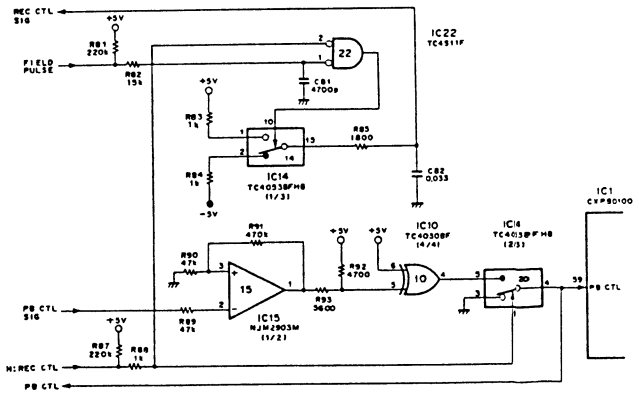



Fig. 5-11. CTL Record/Playback Amplifier

# SECTION 6
# TIME CODE GENERATOR

## 6-1. OUTLINE

The TC-48A board consists of the following circuits:
- TCM (Time Code Module)
- TCMC (Time Code Module Controller)
- System control interface microprocessor
- Display mode selector
- LCD module
- Color frame lock system
- Power backup circuit

## 6-2. TIME CODE GENERATOR

The IC501 is the time code generator IC, and IC502 is the control for the time code generator. The IC503 (CXP80116) is an eight-bit single chip CPU designed to convert the parallel input time code information into serial form and then sent to the SY-117A board.

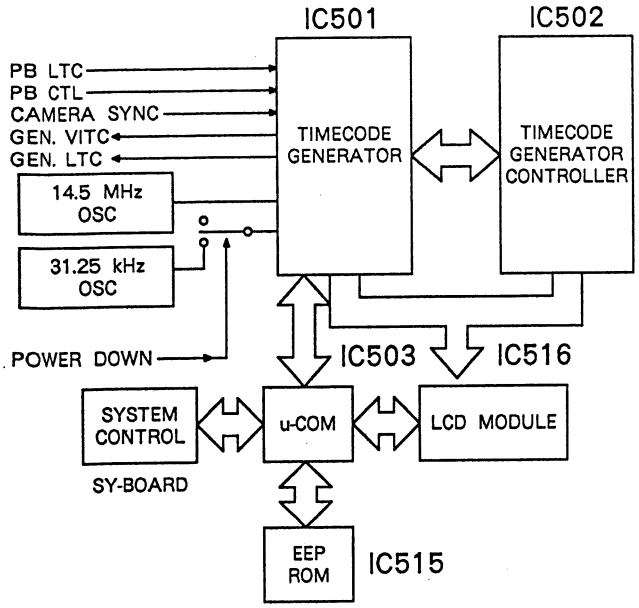



Fig. 6-1. TCG Block Diagram

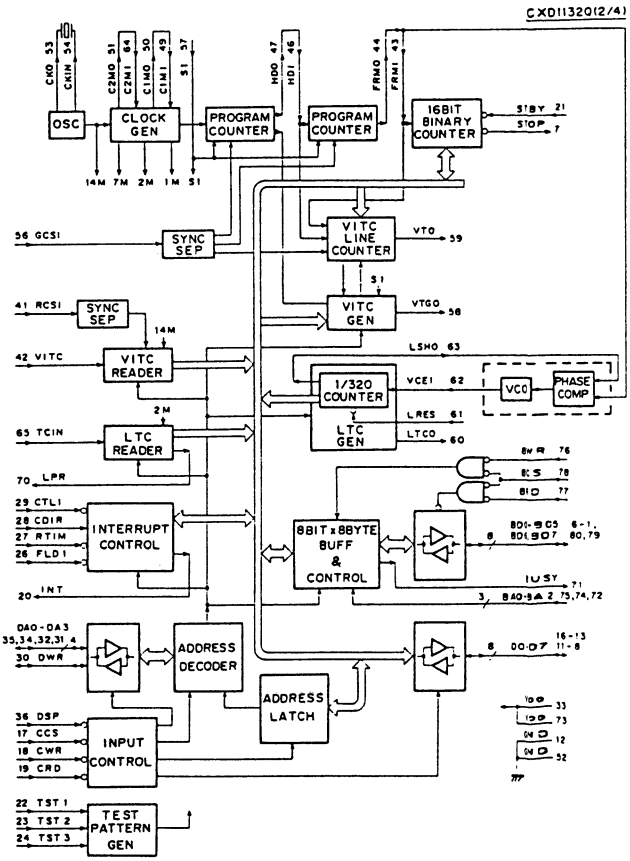
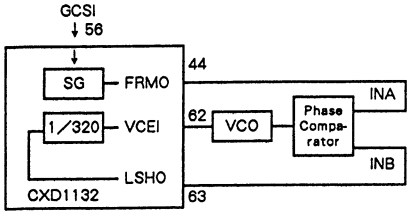
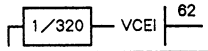
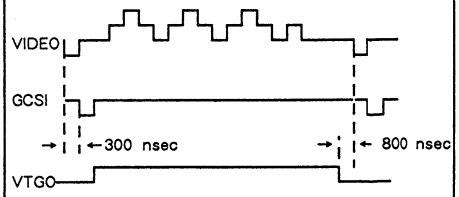



Fig. 6-2. IC501 Block Diagram

# 6-3. OUTLINE OF TIME CODE GENERATOR INPUT/OUTPUT

## Signal Generator

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 54 | I | CKIN | SYSTEM CLOCK IN<br>14.0 to 15.0 MHz is input. The frequency of this clock signal, which is used for frame or signal generation.<br>Signal / CKIN (MHz): SMPTE 29.94 Hz 525 — 14.318; EBU 25 Hz 625 — 14.500 |
| 53 | O | CKO | CLOCK OUT<br>CKIN inverting signal output |
| 55 | I | SLCK | SELECT CLOCK IN<br>Selects the CKIN frequency. CKIN signal is changed to 1/2 by switching to "H".<br>SLCK: "L" / "H"; CKIN: 14.318, 14.500 / 7.159, 7.250 MHz; Standard: SMPTE EBU / SMPTE EBU<br>Current consumption is reduced by generating a 7 MHz signal. Note that with 7 MHz input the VITC reader cannot be used. |
| 56 | I | GCSI | C • SYNC IN<br>Uses reference SYNC IN generator. |
| 48 | O | VDO | VERTICAL SYNC DRIVE OUT<br>Separated VD signal output from GCSI. Usually not used. |
| 47 | O | HDO | HORIZONTAL SYNC DRIVE OUT<br>HD signal output synchronized with GCSI. Connected to pin 46 HDI. |
| 46 | O | HDI | HORIZONTAL SYNC INPUT<br>Connected to pin 47 HDO. |
| 45 | O | GLSY | LOST-SYNC FLAG OUT<br>A "H" signal is output when 4H line or above GCSI signal not input. Usually not used. |
| 44 | O | FRMO | FRAME SIGNAL OUT<br>Frame signal output synchronized with GCSI. Connected to pin 43 FRMI. |
| 43 | O | FRMI | FRAME SIGNAL INPUT<br>Frame signal input. Connected to pin 44 FRMO. |
| 62 | I | VCEI | LTC CLOCK IN<br>Clock signal input used for LTC sync signal generation. The following frequencies are input for the two standards at normal-speed LTC output.<br>LCKI: SMPTE 9.6 kHz; EBU 8.0 kHz |
| 63 | O | LSHO | LTC SYNCHRONOUS SIGNAL H OUT<br>LTC sync signal "H" output. Used to make the output LTC start bit synchronize with the video signal. FRMO, VCEI, and LSHO have the following configuration :<br>  |
| 51 | O | C2MO | CLOCK 2 OUT<br>Divided-by-8 of CKIN (pin 54) output. |

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 49 | I | C1MI | SYSTEM CLOCK IN<br>Connected to C1MO (pin 50). Used as system clock signal. |
| 50 | O | C1MO | CLOCK 1 OUT<br>Divided-by-16 of CKIN (pin 54) output. |
| 61 | I | LRES | LTC COUNTER RESET IN NEGATIVE LOGIC<br>  <br>This counter is reset. |
| 60 | O | LTCO | LTC SIGNAL OUT<br>LTC signal output. The polarity of the LTC output signal is determined by the hot line side of the standard. |
| 59 | O | VTO | VITC SIGNAL OUT<br>VITC signal output. The generation position is different for the SMPTE and EBU standards. In either case, it is generated 500 nsec ahead of the center of the standard. Jitter is 140 nsec for GCSI.<br>It is possible to input VITC at the correct position by making the total of the delay from the input video signal to the GCSI plus the delay until the VITC signal output is mixed with the video signal approx, 500 nsec. |
| 58 | O | VTGO | VITC GATE SIGNAL OUT<br>A "H" level signal is output on the video signal line where VITC is inserted.<br>  |
| 57 | I | S1 | SIGNAL FORMAT SELECT S1<br>Switches according to the signal format.<br>H : NTSC, PAL-M 29.94 Hz 525 lines<br>L : PAL, SECAM 25 Hz 625 lines<br>The output position of the frame generator and VITC signal changes. |

## Longitudinal Time-and-Control Code READER

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 64 | I | C2MI | LTC READ CLOCK IN<br>Input clock signal used for recovering the LTC signal input to TCIN (pin 65).<br>The read range can be altered by changing the frequency of the input clock signal. |
| 65 | I | TCIN | LONGITUDINAL TIME-AND-CONTROL CODE IN<br>Waveform-shaped time code is input at TTL level. |
| 67 | O | DATA | DEMODULATED SERIAL DATA OUT<br>One-bit serial signal output demodulated from the TCIN signal. Used to check the TCIN signal. |
| 66 | O | DCLK | DEMODULATED CLOCK OUT<br>Clock signal output extracted from the TCIN signal. Used to check the TCIN signal. |
| 69 | O | RDSY | READ SYNC WORD DATA OUT<br>SYNC WORD signal output demodulated from the TCIN signal. Output at "H" level during SYNC WORD (bits 64 to 79) period. |
| 68 | O | RFLD | FIELD DATA OUT<br>Bits 0 to 39 of the signal demodulated from the TCIN signal are output at "L" level, and bits 40 to 79 at "H" level. |

## Vertical Interval Time-and Control Code READER

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 42 | I | VITC | VITC SIGNAL IN<br>The VITC signal waveform-shaped to TTL level is input. |
| 39 | I | SLLM | READ SIZE SELECT IN<br>Switching input terminal for setting the readable range for the input VITC signal.<br>"H" level input specifies NTSC : 10 to 30H, PAL/SECAM : 6 (318) to 26 (338) H VITC signal reading. "L" level input specifies all line reading. |
| 38 | O | VRCK | VITC READ CLOCK OUT<br>Input VITC signal read clock signal output. Signal for checking VITC signal. Usually not used. |
| 40 | O | RVDO | VITC READ DATA OUT<br>Input VITC signal read data signal output. Signal for checking VITC signal. Usually not used. |
| 37 | O | DTSE | VITC DATA SEARCH FLAG OUT<br>Reset by V sync signal. Switches to "H" level output when VITC signal is detected. Trigger signal used for checking VITC signal. |
| 41 | I | RCSI | C SYNC IN<br>C sync signal input waveform-shaped to TTL level. |

## External Interface

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 71 | I | BUSY | BUSY OUT<br>H : BUSY<br>L : READY |
| 72<br>74<br>75 | I<br>I<br>I | BA2<br>BA1<br>BA0 | ADDRESS BUS IN |
| 78<br>77<br>76 | I<br>I<br>I | BCS<br>BRD<br>BWR | CHIP ENABLE IN NEGATIVE LOGIC<br>READ IN NEGATIVE LOGIC<br>WRITE IN NEGATIVE LOGIC |
| 79<br>80<br>1<br>2<br>3<br>4<br>5<br>6 | I O<br>I O<br>I O<br>I O<br>I O<br>I O<br>I O<br>I O | BD7<br>BD6<br>BD5<br>BD4<br>BD3<br>BD2<br>BD1<br>BD0 | DATA BUS |

## Time Code Module Control Interface

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 7 | O | STOP | STOP OUT NEGATIVE LOGIC<br>Outputs "L" level signal when the unit enters the standby mode. |
| 70 | O | LPR | LTC READ REQUEST OUT<br>Outputs "H" level signal when LTC data is assembled. |
| 20 | O | INT<br>BRD | INTERRUPT REQUEST OUT<br>Maskable interrupt output signal. |
| 17 | I | CCS | CHIP ENABLE IN NEGATIVE LOGIC<br>Becomes ALE (Address Lock Enable) terminal when DSP terminal is "H" and latches D7-D0. |
| 19<br>18 | I<br>I | CRD<br>CWR | READ IN NEGATIVE LOGIC<br>WRITE IN NEGATIVE LOGIC |
| 8<br>9<br>10<br>11<br>13<br>14<br>15<br>16 | I O<br>I O<br>I O<br>I O<br>I O<br>I O<br>I O<br>I O | BD7<br>BD6<br>BD5<br>BD4<br>BD3<br>BD2<br>BD1<br>BD0 | DATA BUS<br>ADDRESS BUS IN (when DSP terminal is "H") |
| 36 | I | DSP | DISPLAY BUS SELECT IN<br>H : DA0, DA1, DA2, DA3 and DWR become address bus IN.<br>H : CCS terminal becomes ALE (Address Bus Enable).<br>L : DA0, DA1, DA2, DA3 and DWR become address bus OUT. |
| 30<br><br>31<br>32<br>34<br>35 | I<br>O<br>I O<br>I O<br>I O<br>I O | EA4<br>DWR<br>EA3 DA3<br>EA2 DA2<br>EA1 DA1<br>EA0 DA0 | ADDRESS BUS IN NEGATIVE LOGIC<br>WRITE OUT<br>ADDRESS BUS IN/OUT |

## Other Signals

| Pin No. | I/O | Pin Name | Description |
|---|---|---|---|
| 26 | I | FLDI | FIELD REFERENCE INPUT NEGATIVE LOGIC |
| 27 | I | RTIM | TIME ADDRESS RESET INPUT NEGATIVE LOGIC |
| 28 | I | CDIR | CTL DIRECTION INPUT |
| 29 | I | CTLI | CTL SIGNAL INPUT NEGATIVE LOGIC |
| 25 | I | PON | SYSTEM RESET IN NEGATIVE LOGIC<br>Initializes read flag. |
| 21 | I | STBY | STANDBY READ FLAG NEGATIVE LOGIC<br>Readable flag from TMC. STOP signal can be output when low. |
| 22<br>23<br>24 | I<br>I<br>I | TST1<br>TST2<br>TST3 | TEST IN<br>Test input terminals. Connected to Vss (GND). |
| 33<br>73 | I<br>I | $V_{DD}$ | POWER LINE<br>A supply voltage of +4.25 to +5.25V is input. |
| 12<br>52 | O<br>O | Vss | GND LINE<br>Connected to GND (0V). |

## 6-4. DISPLAY MODE SELECTOR

Because the TC-48A board of this equipment has the same circuit configuration of the BVV-5PS series VTR time code circuit, description is given only to the newly added switches.

(1) S517 (SLAVE LOCK INT/EXT switch)
This switch determines whether the user bit of internal time code is used or the user bit of external time code is used during the slave lock mode. When shipped from the factory, the switch is set to INT.

(2) S518 (RT VITC/LTC switch)
This switch is used when user bit is inserted into VITC and the real time is inserted into LTC. When shipped from factory, real time is inserted into VITC.

(3) DIAGNOSTIC switch
When this switch is pressed once, the self-diagnostic mode is entered. Self diagnostics can then be performed using the ADVANCE and SHIFT switches.

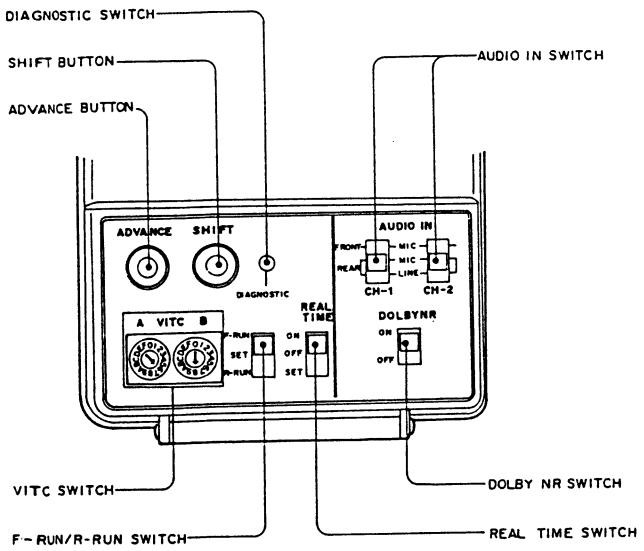



Fig. 6-3. Switch Location Diagram

## 6-5. LCD

The LCD (IC516) has built-in LCD driver and LCD display. Data is displayed by using the following two ICs.

- CXD-1128Q : Time code driver
- MSM5219B : Battery/audio level display, indicator digital display and alarm.

The battery level indicating voltage is supplied from the PS-162 board to the TC-48A board, and is sent to pin 50 of IC503 through a level shifter amplifier. It is then A/D converted into a 8-bit digital data to be displayed on the LCD. The audio CH-1 and CH-2 level voltages are sent to pins 49 and 48 of IC503 respectively, and these signals are also A/D converted and displayed on the LCD.
Content of the hours meter can be displayed when the self-diagnostic mode is established. The hours meter calculates the elapsed time by applying interrupt with vertical sync signal that is obtained by separating it from the composite sync signal using IC503. The number of interrupt is counted. The hours meter displays the following three informations.

- Accumulated hours of head drum rotation
- Accumulated hours of tape running
- Accumulated hours of equipment power ON

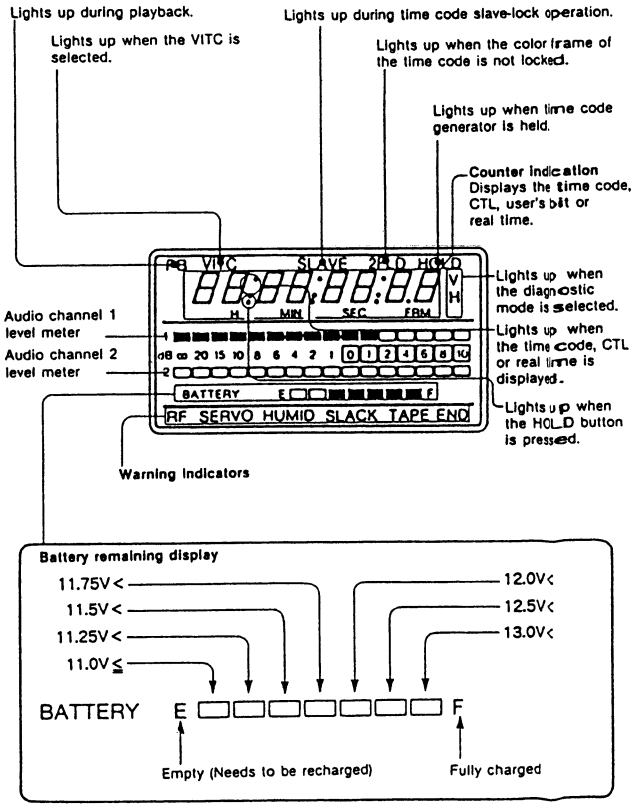

Lights up during playback.
Lights up during time code slave-lock operation.
Lights up when the VITC is selected.
Lights up when the color frame of the time code is not locked.
Lights up when time code generator is held.
Counter indication
Displays the time code, CTL, user's bit or real time.
REC VITC SLAVE 2FLD HOLD
H MIN SEC FRM V H
Lights up when the diagnostic mode is selected.
Audio channel 1 level meter
Audio channel 2 level meter
Lights up when the time code, CTL or real time is displayed.
BATTERY E F
RF SERVO HUMID SLACK TAPE END
Lights up when the HOLD button is pressed.
Warning Indicators
Battery remaining display
11.75V<
11.5V<
11.25V<
11.0V≦
12.0V<
12.5V<
13.0V<
BATTERY E F
Empty (Needs to be recharged)
Fully charged

Fig. 6-4. LCD

## 6-6. COLOR FRAME LOCK SYSTEM

In this equipment, the frame reference pulse is sent to pin 26 of IC501 (TCM) so that time code signal is locked to the color frame of the chroma signal.

## 6-7. POWER BACKUP CIRCUIT

The TC-48A board has three power supply systems.

(1) +5V power supply that is locked to the power switch ON/OFF operation.
This is the +5V power supply that is fed when the power switch is operated.

(2) BATT +5V
The BATT +5V is the power supply that keeps providing power to the CPU (IC503) and non-volatile memory (IC515) for approximately 2.6 seconds even after the power switch is turned OFF. The capacitor C4 (0.33F) on the PS-162 board is the capacitor for back-up power. By this power supply, data can be written down into non-volatile memory (IC515) within approximately 2.6 second period.

(3) TC +5V
The time code signal can be backed-up for approximately 18 minutes by the capacitor C520 (1F) even after the battery is extracted.
If the battery should be removed, the standby command ("Low" level) is input to pin 21 of IC501 and the stop command ("L") is output from pin 7. This stop command is sent to pin 57 of IC502 to stop operation of IC502. This signal is also sent to pin 10 of IC516 (LCD) to stop operation of the LCD. When the battery is extracted, crystal oscillators X501 and X502 stop oscillating. Only X503 continues oscillating at 2fH in order to backs up the time code for 18 minutes. Also, in order to prevent erroneous operation of IC501, IC505 detects the power supply voltage during power backup mode. If the power voltage drops below 3V, IC501 is reset forcibly.
Since C554 (1F) and C555 (1F) have been connected in parallel with C520 in order to extend the back up time and to reduce the power consumption, however, back up time becomes five years or more by using lithium battery at present. C520 still remains in order to keep the back up time for about 18 minutes after discharging the lithium.

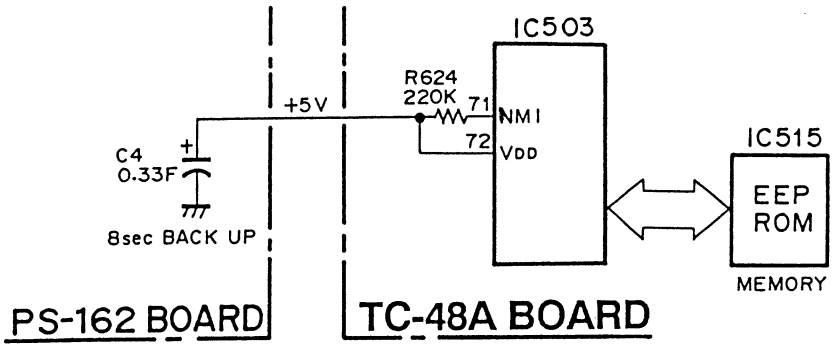



Fig. 6-5. Memory Back-up

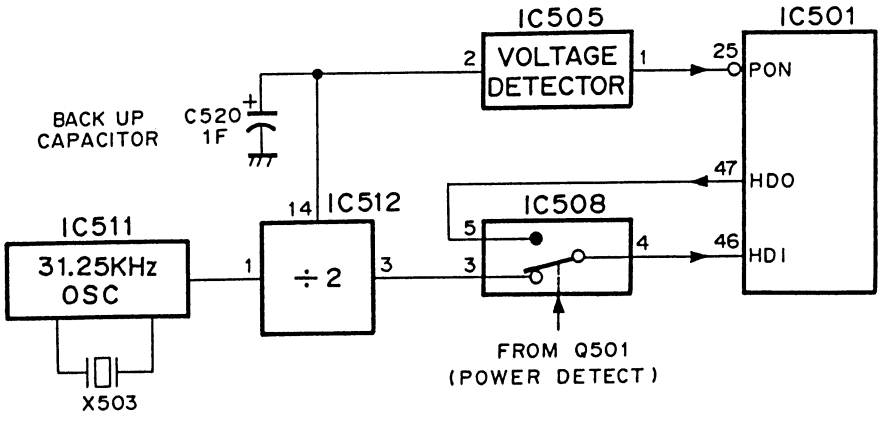



Fig. 6-6. TC Back-up

## 6-8. PLL CIRCUIT

The IC509 forms a PLL circuit. The composite sync signal that is supplied from the SG-152 board on the camera block, is sent to the phase comparator circuit pin 56 of IC501, and the comparator output is sent to VCO. The VCO oscillates at the frequency depending upon the all voltage. The VCO output is sent to IC501 where it is divided by 320 and is fed-back to IC509 phase comparator. By this PLL circuit, the time code that is synchronized with the SG-152 board on the camera block output sync, is generated. When power is turned OFF, composite sync signal will not come, so that the time code signal is generated by self-running of IC501.

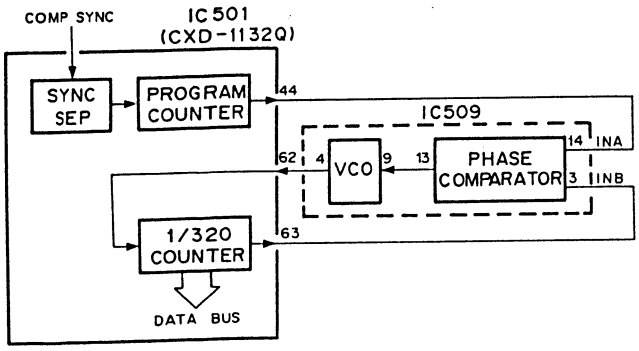



Fig. 6-7. PLL Circuit

## 6-9. NON-VOLATILE MEMORY

IC515 is the non-volatile memory that is used to back-up the hours meter related data. When power is turned OFF, the hours meter data is written from IC503 to IC515. When power is turned ON, the data stored in IC515 is retrieved. The battery-before-alarm data and the users bit data are also backed-up as well by this non-volatile memory.

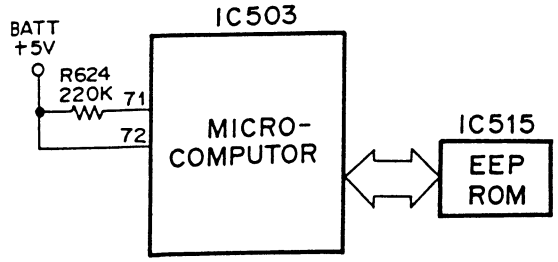



Fig. 6-8. Non-volatile Memory

## 6-10. RESET CIRCUIT

When the CPU (IC503) is reset, the pin 2 of IC517 is forced to go to "H" level by the CPU so that the other reset is inhibited. At the same time, Q504 is set to ON by pin 4 of IC503 output that discharges C547 charge. As data must be written into non-volatile memory when power is turned OFF, the data is written during this period with +5V battery.

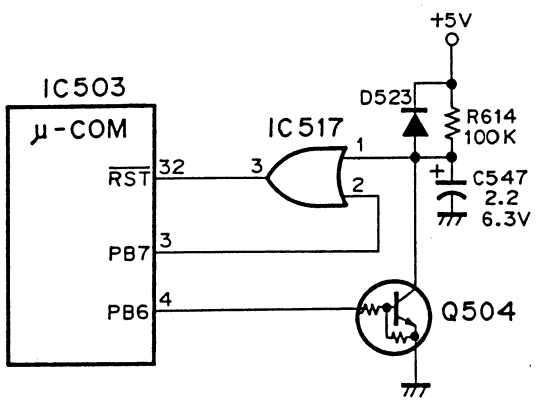



Fig. 6-9. Reset Circuit

## 6-11. TIME CODE SLAVE LOCK CIRCUIT

When the time code is input to TC IN at pin 65 of IC501, a "READ SYNC WORD" signal is output from RDSY of pin 69. However, this "READ SYNC WORD" signal is output during playback mode too, it is necessary that it should not be slave-locked by the time code during playback mode. Therefore, in order to ensure this, sets pin 10 of IC502 to "H" so that slave lock is inhibited even though time code is supplied to IC501.

When time code signal is supplied from external source, the monostable multivibrator IC513 is triggered to set IC506 and the "L" level is output from pin 15 of analog switcher IC508. Though pin 10 of IC502 becomes to "L" and slave lock is engaged. When slave lock is engaged, the time code signal TCI supplied from pin 2 of CN2 to IC501 has priority and is used.

In order to release the slave lock, there two ways as follows :

- Reset the system of IC501.
- Set REC RUN/SET/FREE RUN switch to REC RUN or SET position.

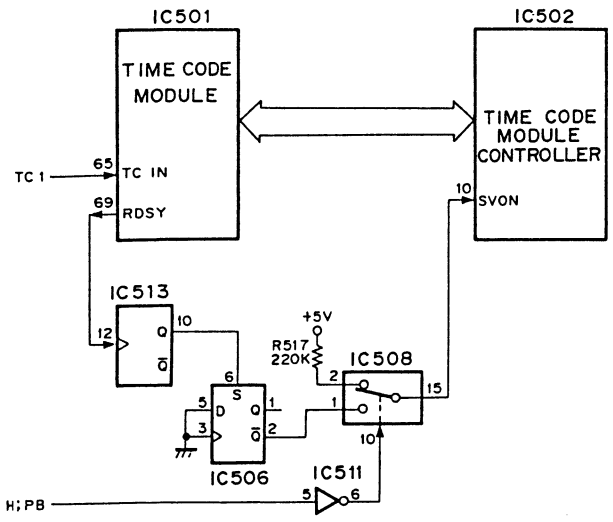



Fig. 6-10. Time Code Slave Lock Circuit

## 6-12. REAL TIME SET CIRCUIT

When shipped from factory, the real time (R TIME) is inserted in the VITC's users bit. The real time can be seen by setting the REAL TIME switch to SET position. The real time is not displayed when the REAL TIME switch is set to OFF or ON positions. Also, if the REAL TIME switch is simply set to SET position, the real time will stop. Therefore, by the circuit composed of IC507, that makes possible to confirm the real time when HOLD button is pressed with the DISPLAY switch is set in the U-BIT position. This circuit allows viewing the real time value as long as the HOLD button is pressed down.

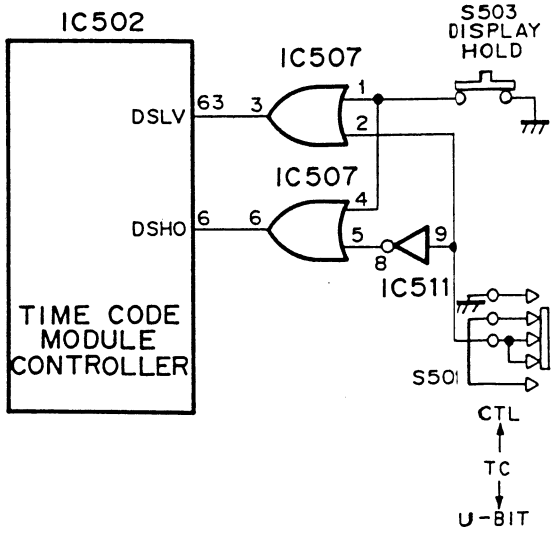



Fig. 6-11. Real Time Set Circuit

## 6-13. SELF DIAGNOSTIC MODE

The VTR goes into the self diagnostic mode when DIAGNOSTIC switch S513 is pressed. When S513 is pressed, pin 5 of IC503 goes to "H" level, pins 8 and 11 of IC517 are forced to PRESET state and pins 4 and 5 are set to H level. This ensures that pressing the ADVANCE switch or the SHIFT switch during the self diagnostics mode will not have no adverse effect on the time code.

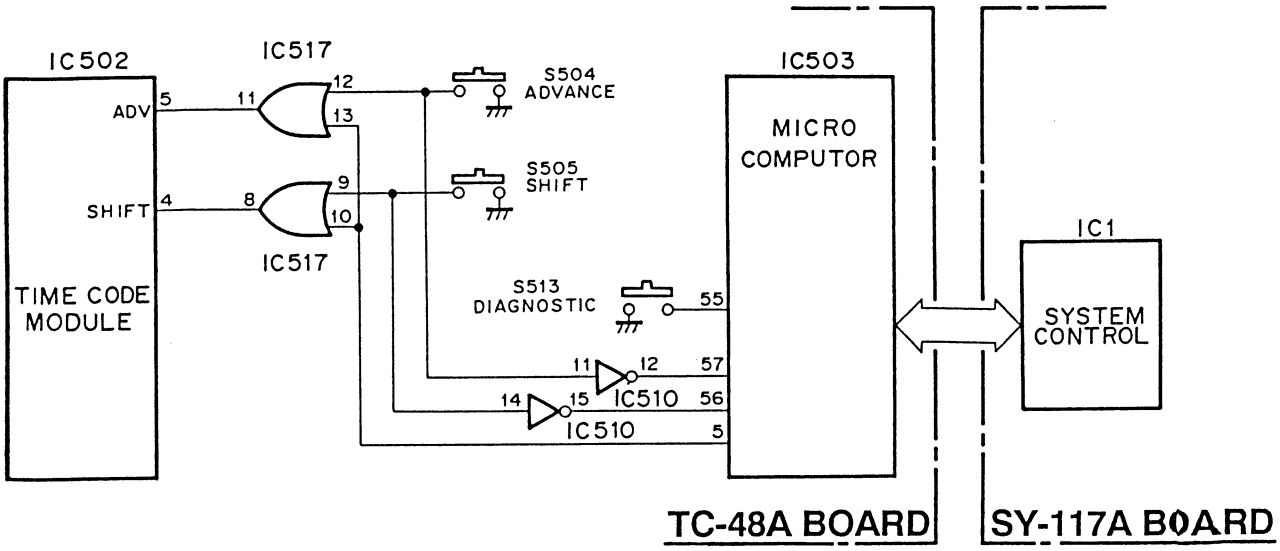



Fig. 6-12. Simple Block Diagram during Self-diagnostics Mode

# SECTION 7
# INTERFACE OF THE BVW-35P/25P

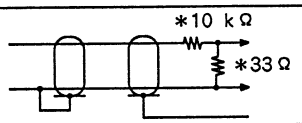
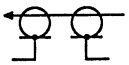
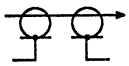
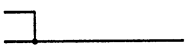
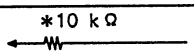
## 7-1. OUTLINE

In the BVW-300P, when connecting the 20P connector for the playback adaptor to the BVW-35P/25P with exclusive cable (CCRZ-5), the signal (composite signal only) from the camera can be recorded to the BVW-35P/25P by pressing the VTR START switch on the BVW-300P.

## 7-2. INTERFACE SPECIFICATIONS AND CIRCUITS

PB ADAPTOR Connector (20P)

- In case when connecting the BVW-35P/25P with optional connecting cable CCRZ-5.

| No. | SIGNAL | REMARKS FOR SIGNAL | DIRECTION | BVW-35P/25P 26pin No. |
|---|---|---|---|---|
| 1 | W35P REC/ALARM IN | 0V, +2.5V, +5 Vdc | ← | 15 |
| 20 | W35P START/STOP | START : 4.5 Vdc<br>STOP : 0 Vdc | → | 12 |
| 3 | AUDIO CH1 (X) OUT | Output −10 dBu |  | 9 |
| 4 | AUDIO CH1 (G) OUT | | | 10<br>11 |
| 18 | RETURN VIDEO (X) IN | 1.0 Vp-p, 75Ω |  | 18 |
| 15 | RETURN VIDEO (G) IN | | | 19 |
| 9 | VIDEO OUT (X) | 1.0 Vp-p, 75Ω |  | 1 |
| 10 | VIDEO OUT (G) | | | 2 |
| 7 | GND | |  | B |
| 8 | GND | | | |
| 12 | INTERFACE SENCE | UNREG +12V IN |  | A |

*The CCRZ-5 cable includes three resistors.

**Table 7-1. Signal Contents when Connecting the BVW-35P/25P**

A circuit related to an above functions are mounted on the MB-173A board.
When connecting the BVW-35P/25P, UNREG +12V is input to pin 2 of IC401 through 10 kΩ resistor inside the cable and pin 1 becomes to Low level. This state is fed to pin 19 of IC1 through pin 49 of connector on the SY-117A board, VTR section of the BVW-300P is set into the SAVE mode and operations other than EJECT and LOADING are inhibited.
When depressing the VTR START switch and the trigger is input to pin 2 of IC402, High level is output from pin 4 and the BVW-35P/25P will go into the recording mode.

A REC TALLY signal from the BVW-35P/25P is input to pin 7 of IC402 where it is level-shifted and output from pin 5. This signal is used as REC/ALARM signal after passing through IC401, Q2 and Q1.
During depressing the RET (RETURN) switch on the lens block, pins 2 and 15 of IC2 conducts and the PB video signal can be observed on the viewfinder when the PB video signal is input from the BVW-35P/25P. Q403 is used for eliminating a cross-talk of IC2.

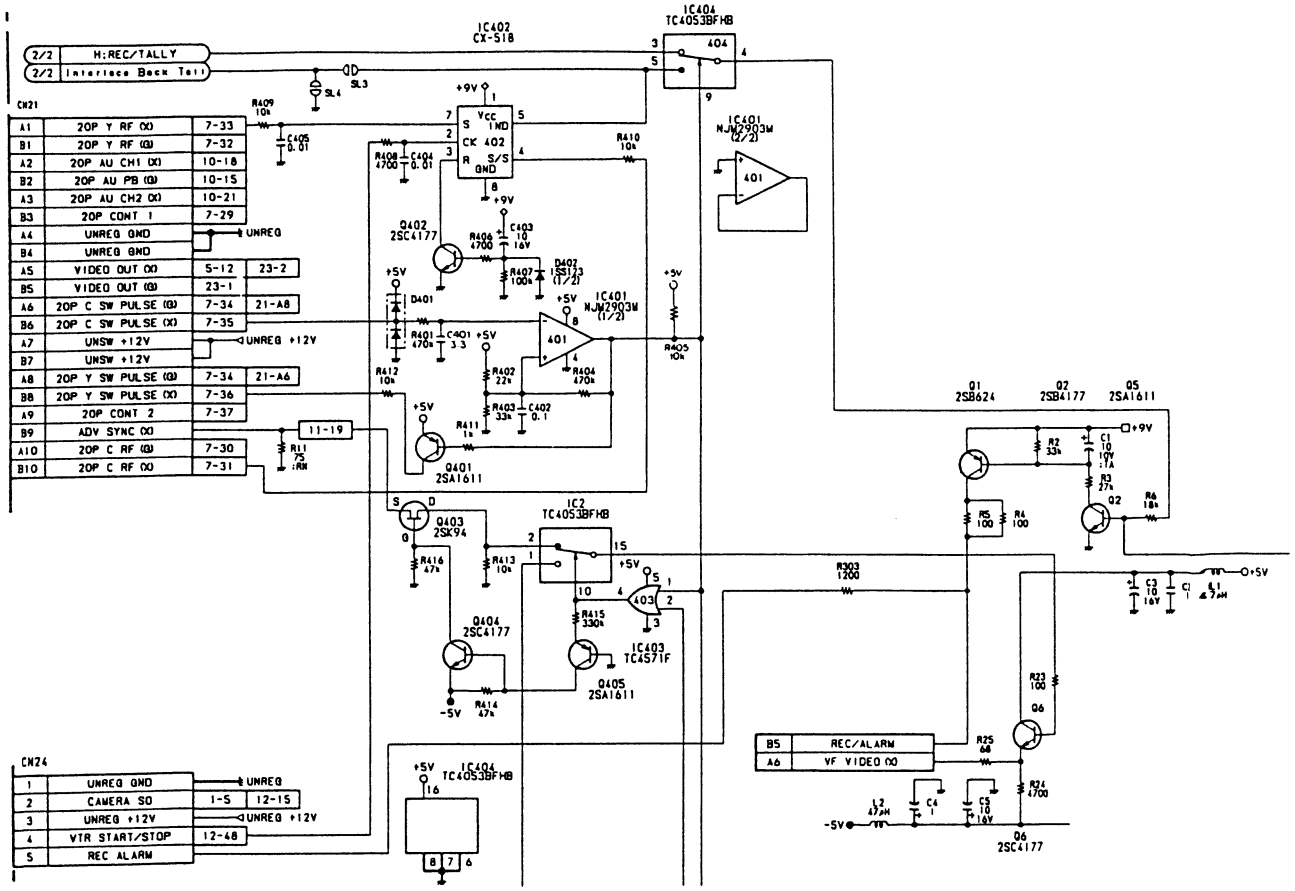



Fig. 7-1. Interface Circuit for the BVW-35P/25P